GREEN TECHNOLOGY -
A NEW ERA FOR ELECTRONICS

Polynomial Complexity Asynchronous Control Circuit Synthesis of Concurrent Specifications based on Burst-Mode FSM Decomposition

Pavlos M. Mattheakis
Christos P. Sotiriou

26th International Conference on VLSI
January 2013
Pune,India

TSI

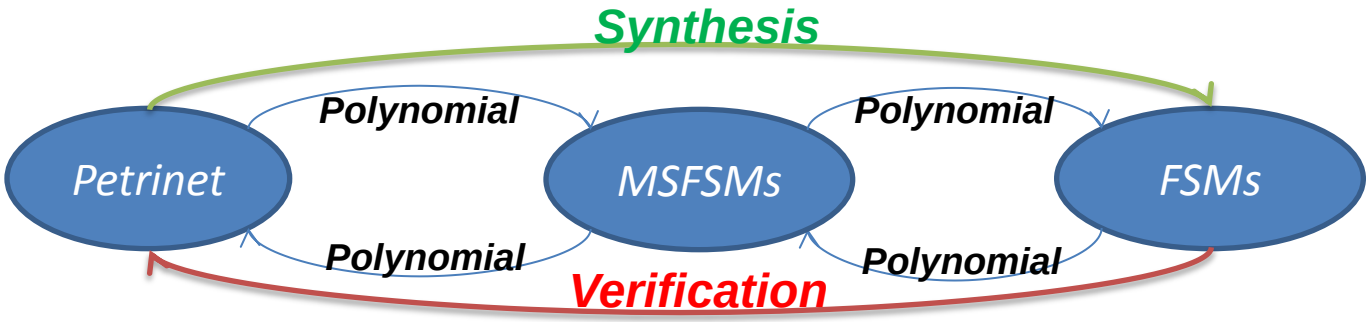
FORTH
Institute of Computer Science

Overview

- ***Aim of this work***
- Petrinet Operation
- Asynchronous Circuits Implementation Flows
- Proposed Flow
- Results
- Conclusion and Future Work

Multiple Synchronized FSMs

- Novel Model for Concurrent Control Specifications
  - Parallel Tasks Described with FSMs
  - Synchronization explicitly described
    - Transition Barriers, Wait States
  - Polynomial Implementation and Verification Paths



*Mattheakis, Pavlos M., Christos P. Sotiriou, and Peter A. Beerel. "A polynomial time flow for implementing Free-Choice Petri-nets." *Computer Design (ICCD), 2012 IEEE 30th International Conference on*. IEEE, 2012.

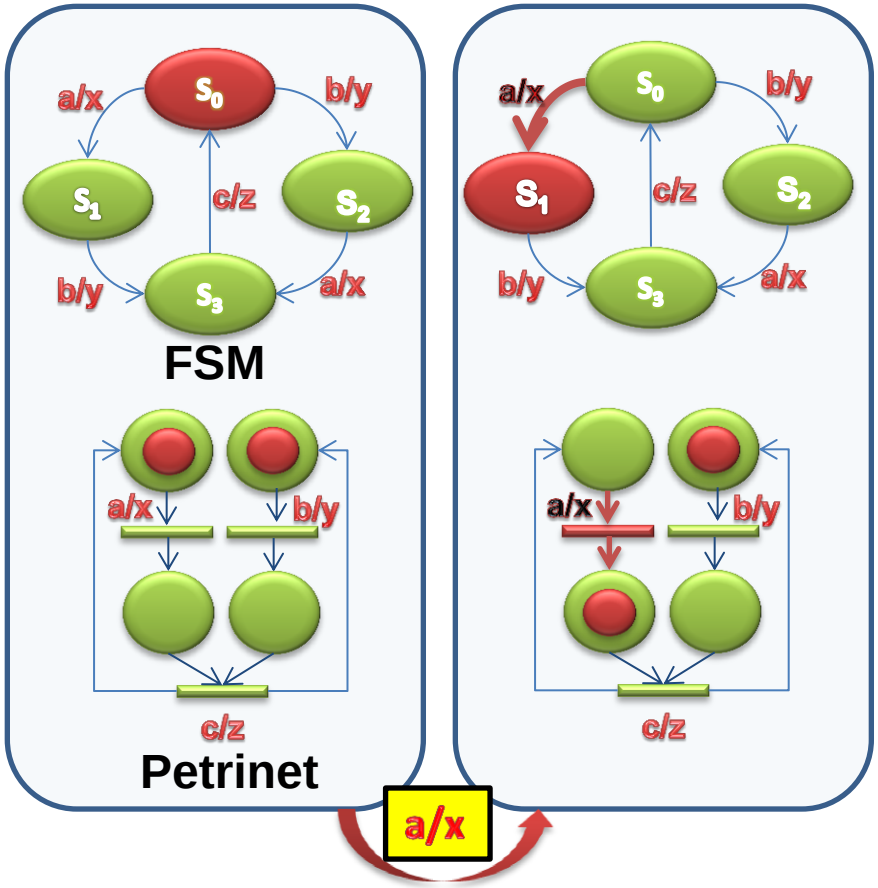
Aim of this Work

- Use MSFSMs as a vehicle to synthesize Asynchronous Circuits
  - Transform PTNets to legal BM-FSMs
  - Use FSM-oriented mature algorithms to examine the solution space
- Introduce a Scalable Logic Synthesis Tool
  - Low Execution Time
  - High Quality Results

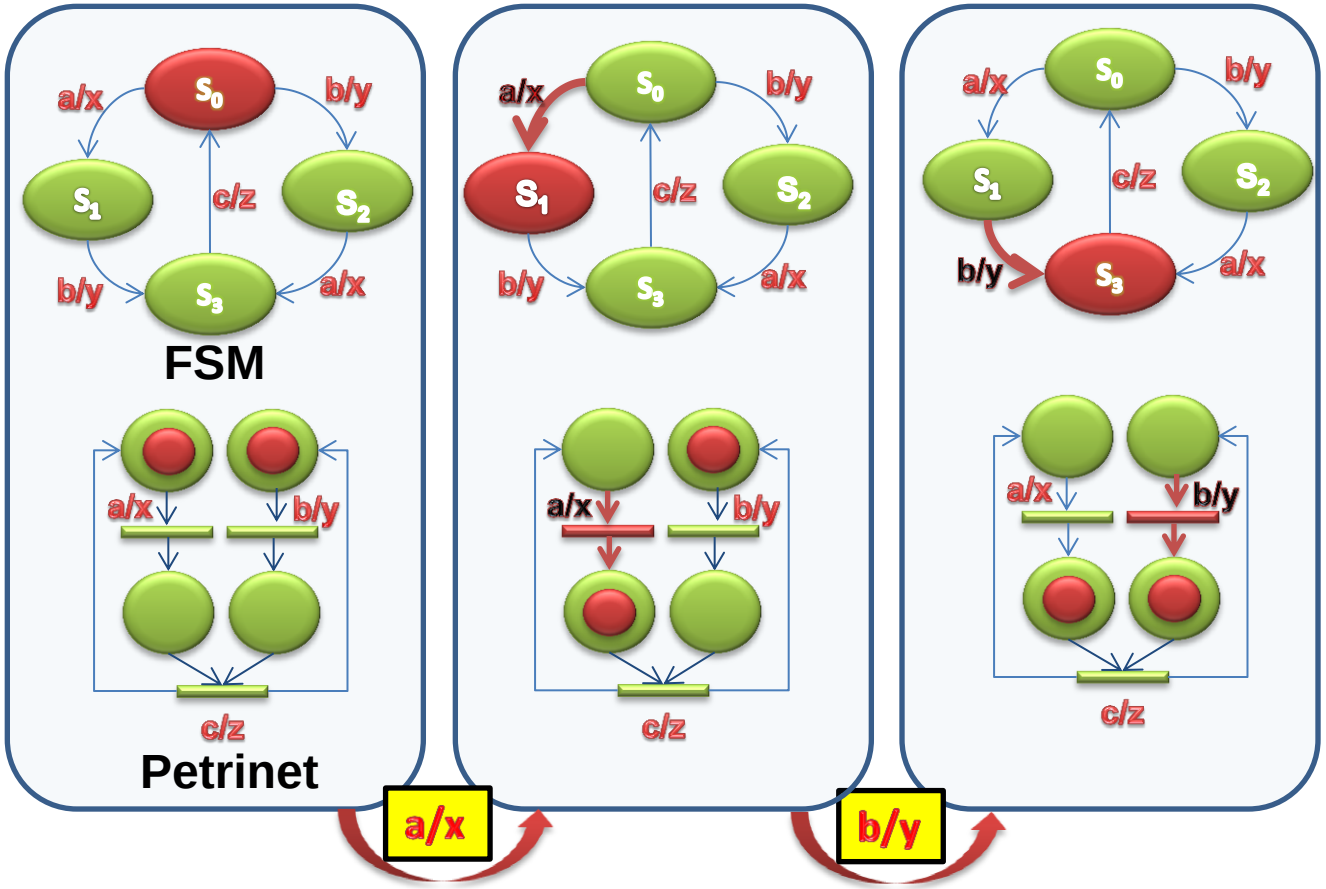
Overview

- Aim of this work
- ***Petrinet Operation***
- Asynchronous Circuits Implementation Flows
- Proposed Flow
- Results
- Conclusion and Future Work

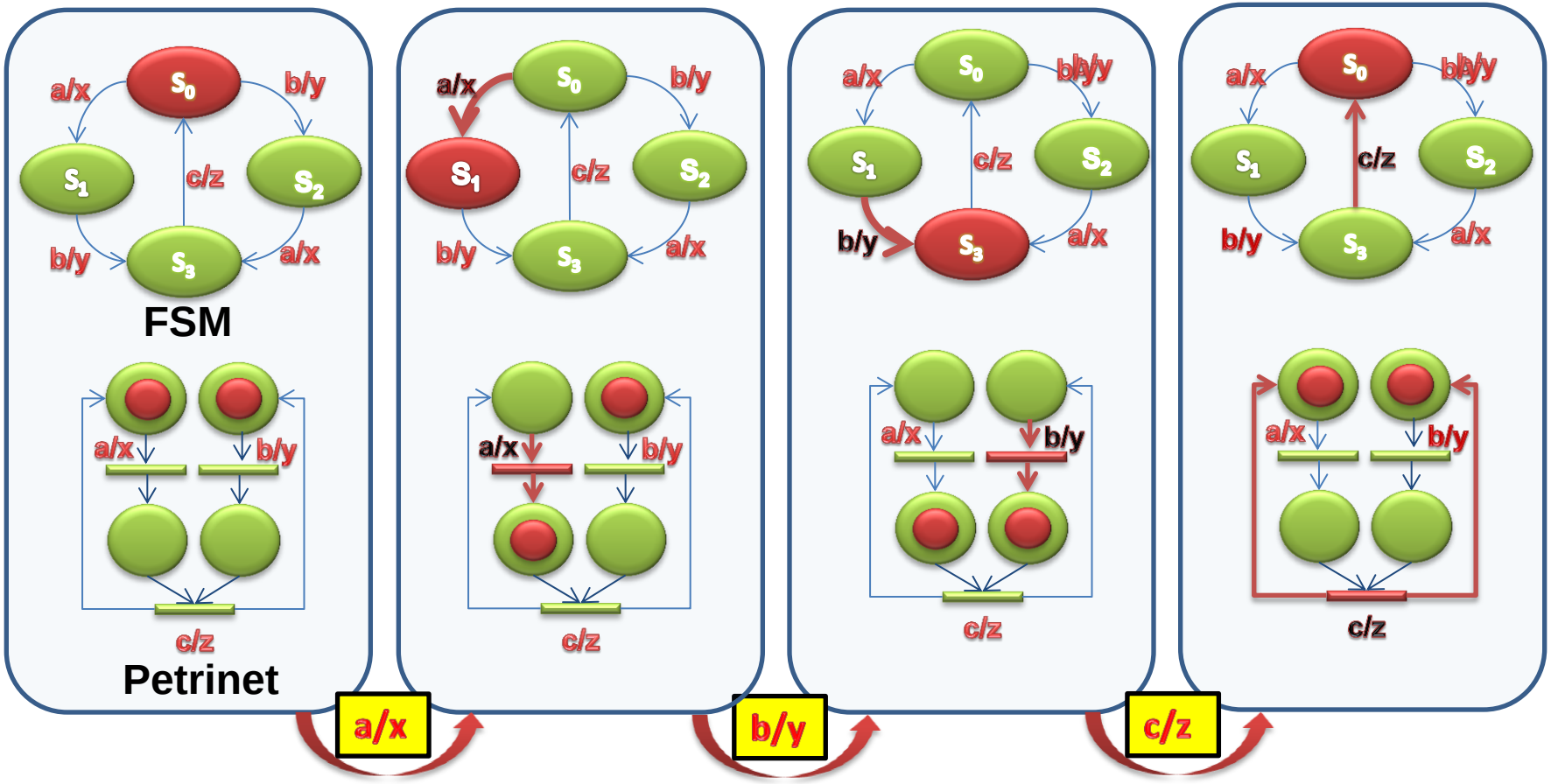
Petrinet Operation



Petrinet Operation



Petrinet Operation



Overview

- Aim of this work
- Petrinet Operation
- ***Asynchronous Circuits Implementation Flows***
- Proposed Flow
- Results
- Conclusion and Future Work

Asynchronous Circuits Implementation Flows

(A)(BM)FSM Synthesis*	Petrinet Synthesis#	Direct Mapping~
• Conventional FSM Heuristics • Exponential Concurrent Specifications	• Compact Concurrent Specifications • Exponential Synthesis Time	• Linear Synthesis Time • Suboptimal Results

*Kenneth Y. Yun and David L. Dill, *"Automatic synthesis of extended burst-mode circuits"*, IEEE TCAD, 1999

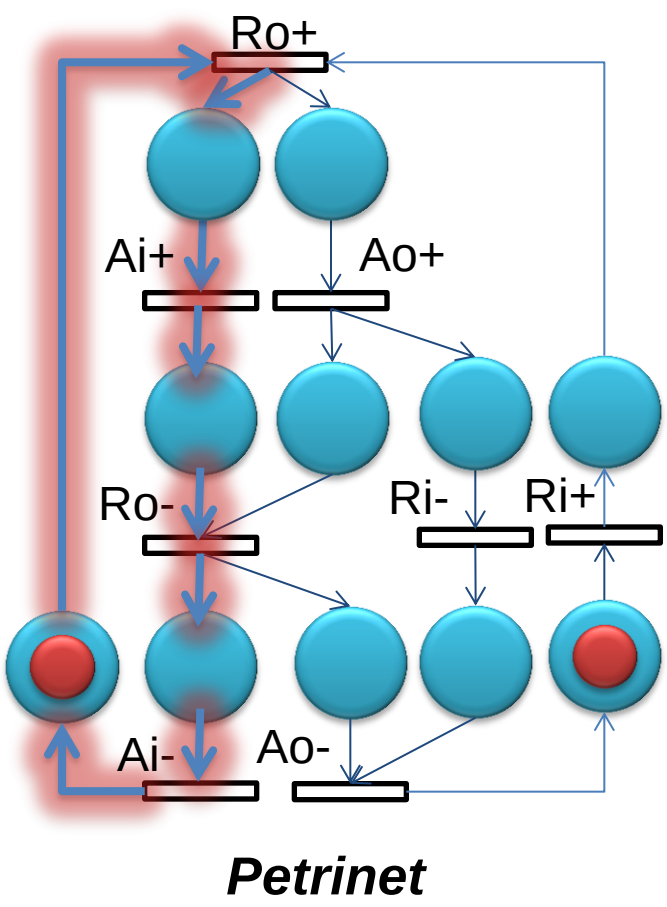
#J. Cortadella et al., *"Logic Synthesis of Asynchronous Controllers and Interfaces"*, Springer-Verlag, 2002.

~D. Sokolov, A. V. Bystrov, and A. Yakovlev, *"Direct Mapping of Low-Latency Asynchronous Controllers from STGs,"* IEEE TCAD, 2007

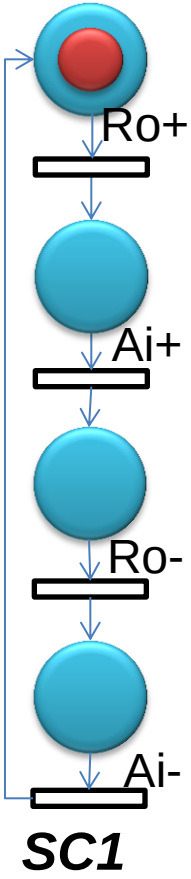
Overview

- Aim of this work
- Petrinet Operation
- Asynchronous Circuits Implementation Flows
- ***Proposed Flow***
- Results
- Conclusion and Future Work

Handshake Controller (1/4)



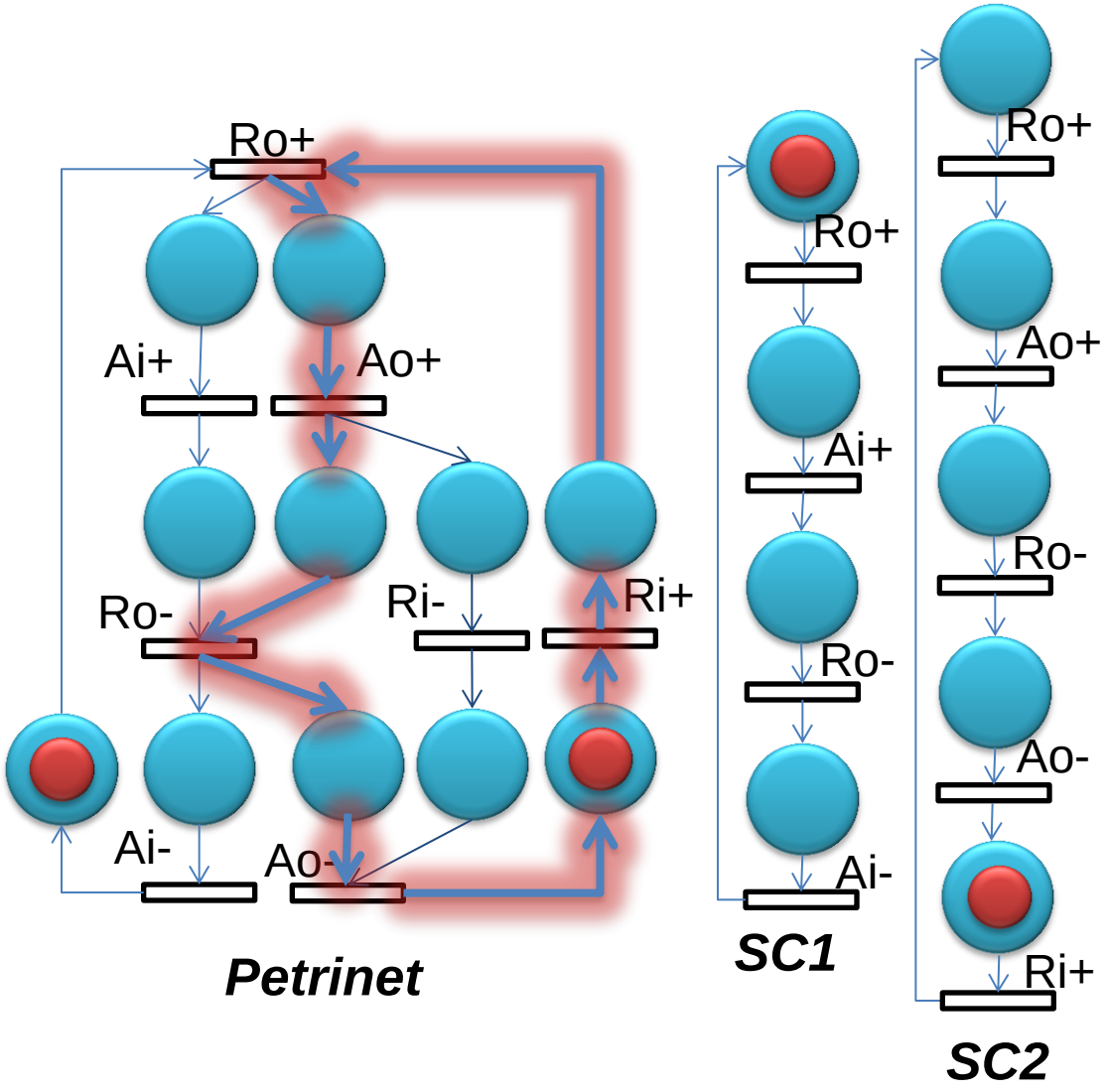
Petrinet



SC1

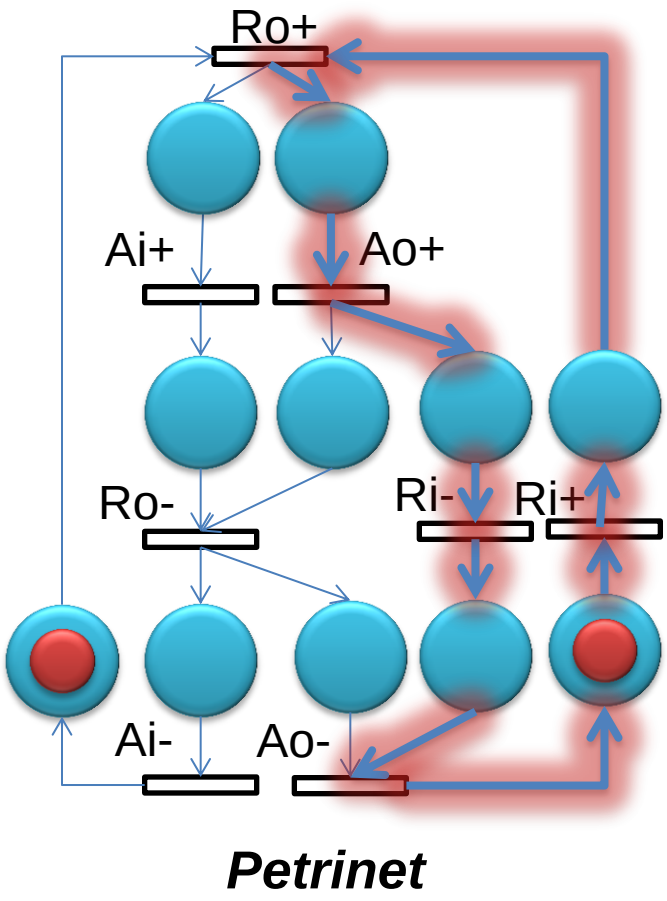
- Petrinet to S-Component Decomposition
- S-Component to BM-FSM Mapping
- Synchronization Primitive Extraction
- Synchronization Integration

Handshake Controller (1/4)

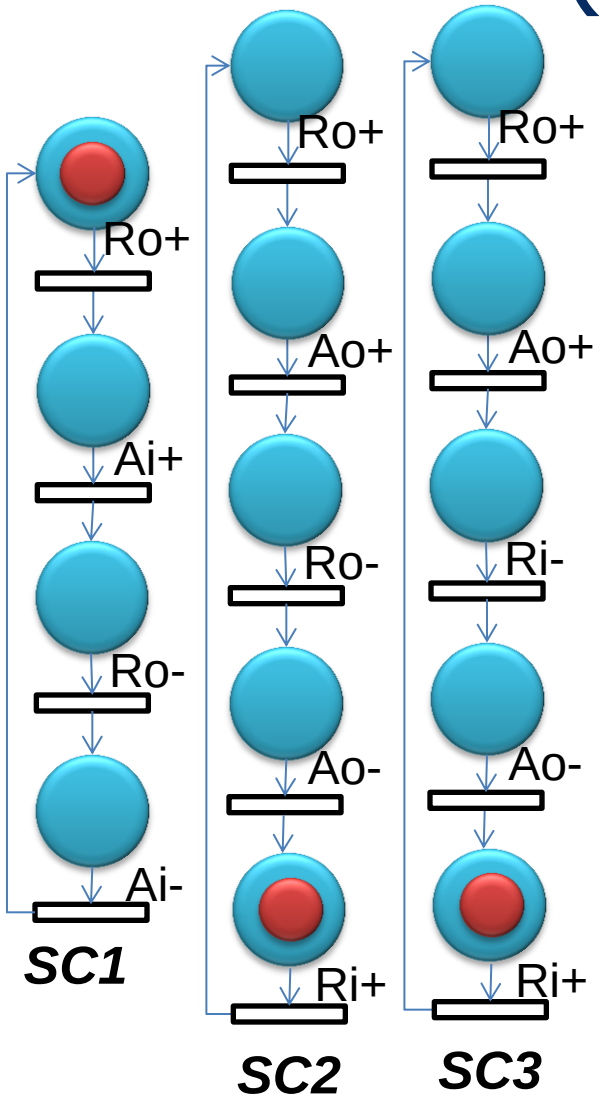


- Petrinet to S-Component Decomposition
- S-Component to FSM Mapping
- Synchronization Primitive Extraction
- Synchronization Integration

Handshake Controller (1/4)

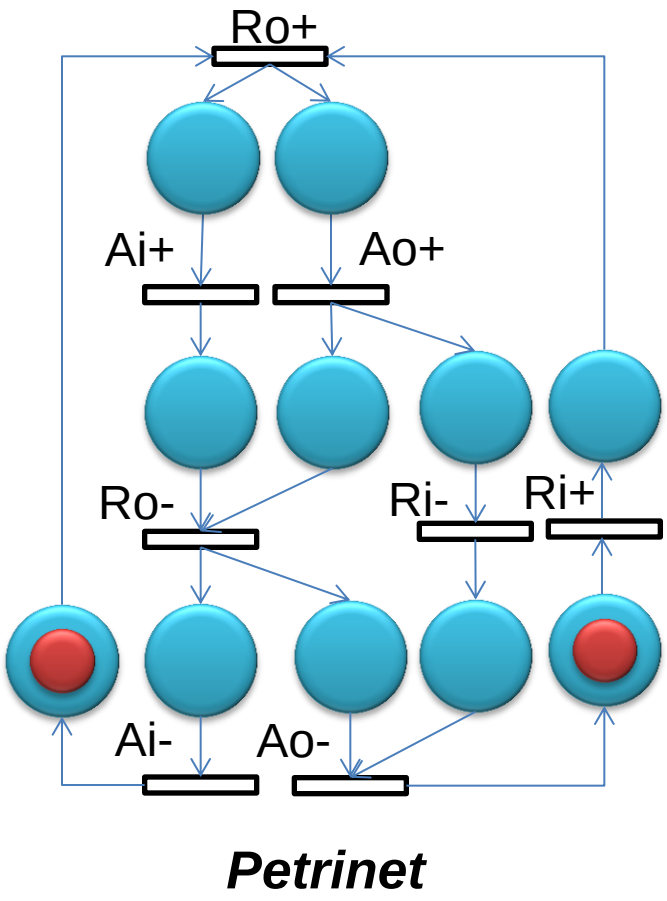


Petrinet

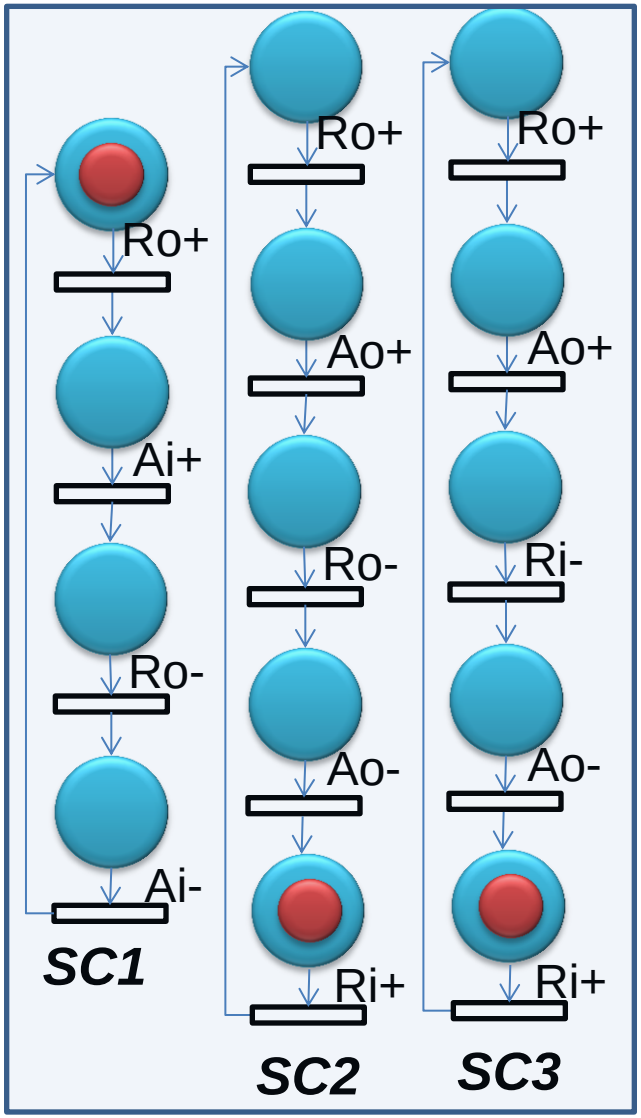


- Petrinet to S-Component Decomposition
- S-Component to BM-FSM Mapping
- Synchronization Primitive Extraction
- Synchronization Integration

Handshake Controller (1/4)



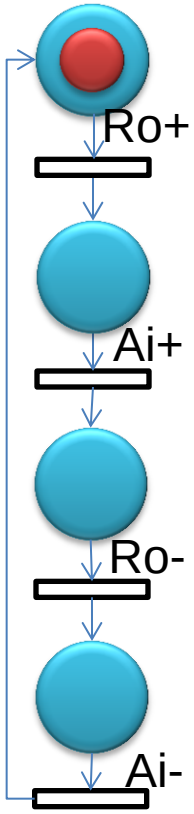
Petrinet



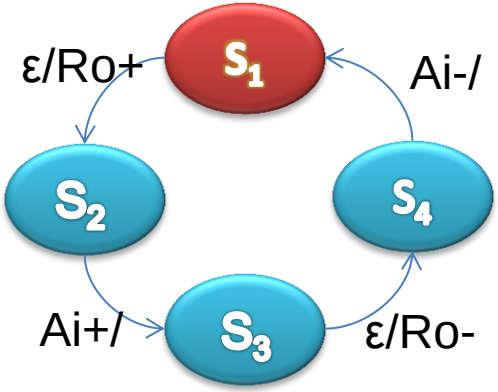
SCover

- Petrinet to S-Component Decomposition
- S-Component to BM-FSM Mapping
- Synchronization Primitive Extraction
- Synchronization Integration

Handshake Controller (2/4)



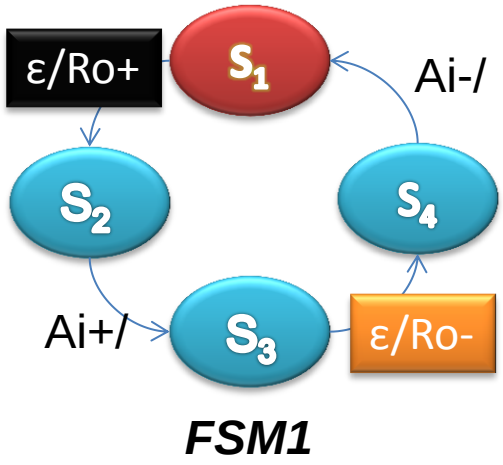
SC1



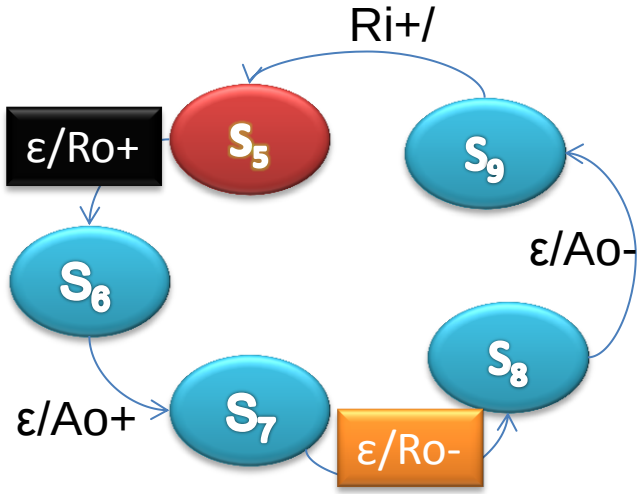
FSM1

- Petrinet to S-Component Decomposition
- S-Component to BM-FSM Mapping
- Synchronization Primitive Extraction
- Synchronization Integration

Handshake Controller (3/4)

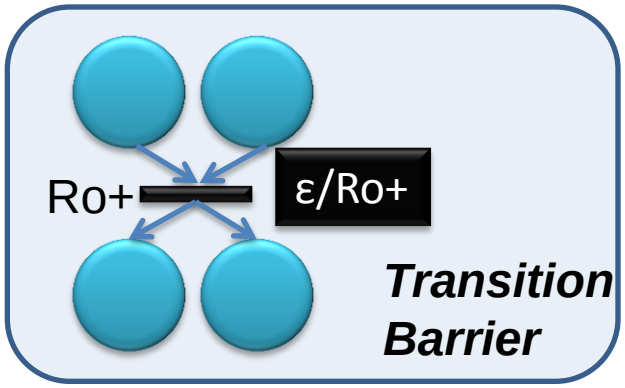


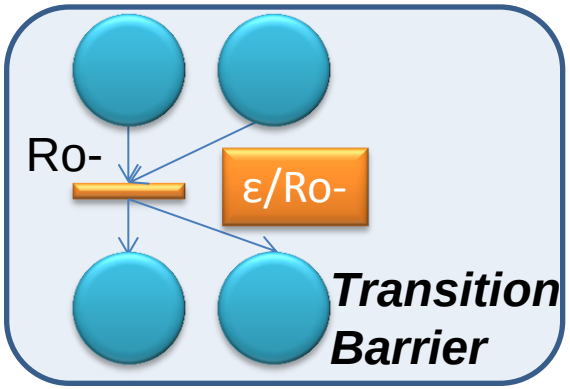
FSM1



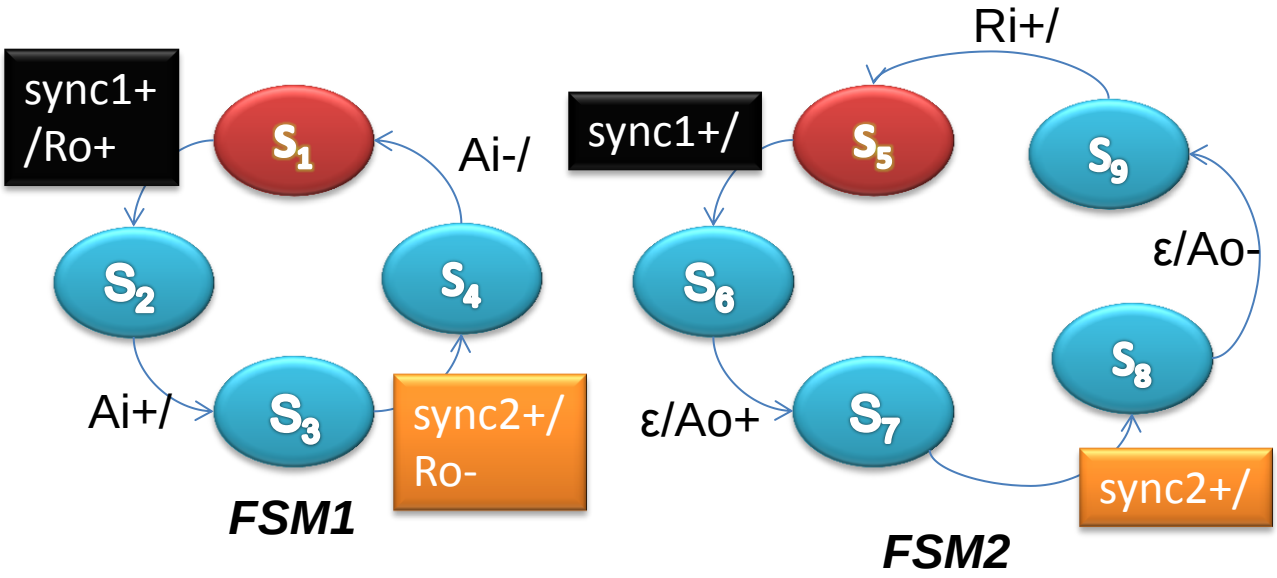
FSM2

- Petrinet to S-Component Decomposition
- S-Component to FSM Mapping
- Synchronization Primitive Extraction
- Synchronization Integration





Handshake Controller (4/4)

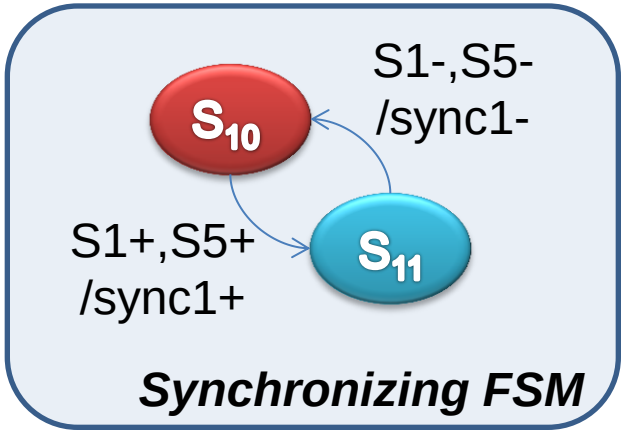


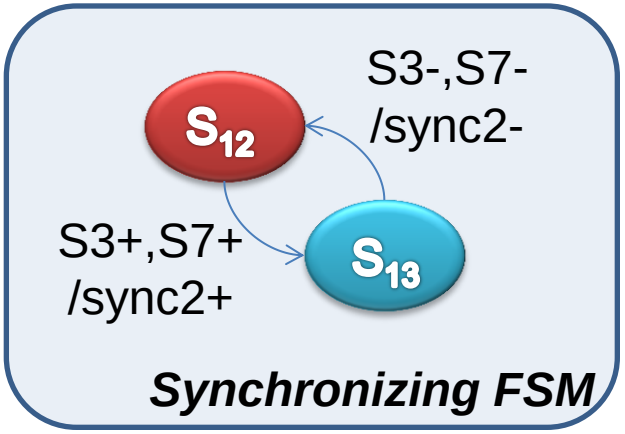
Petrinet to S-Component Decomposition

S-Component to FSM Mapping

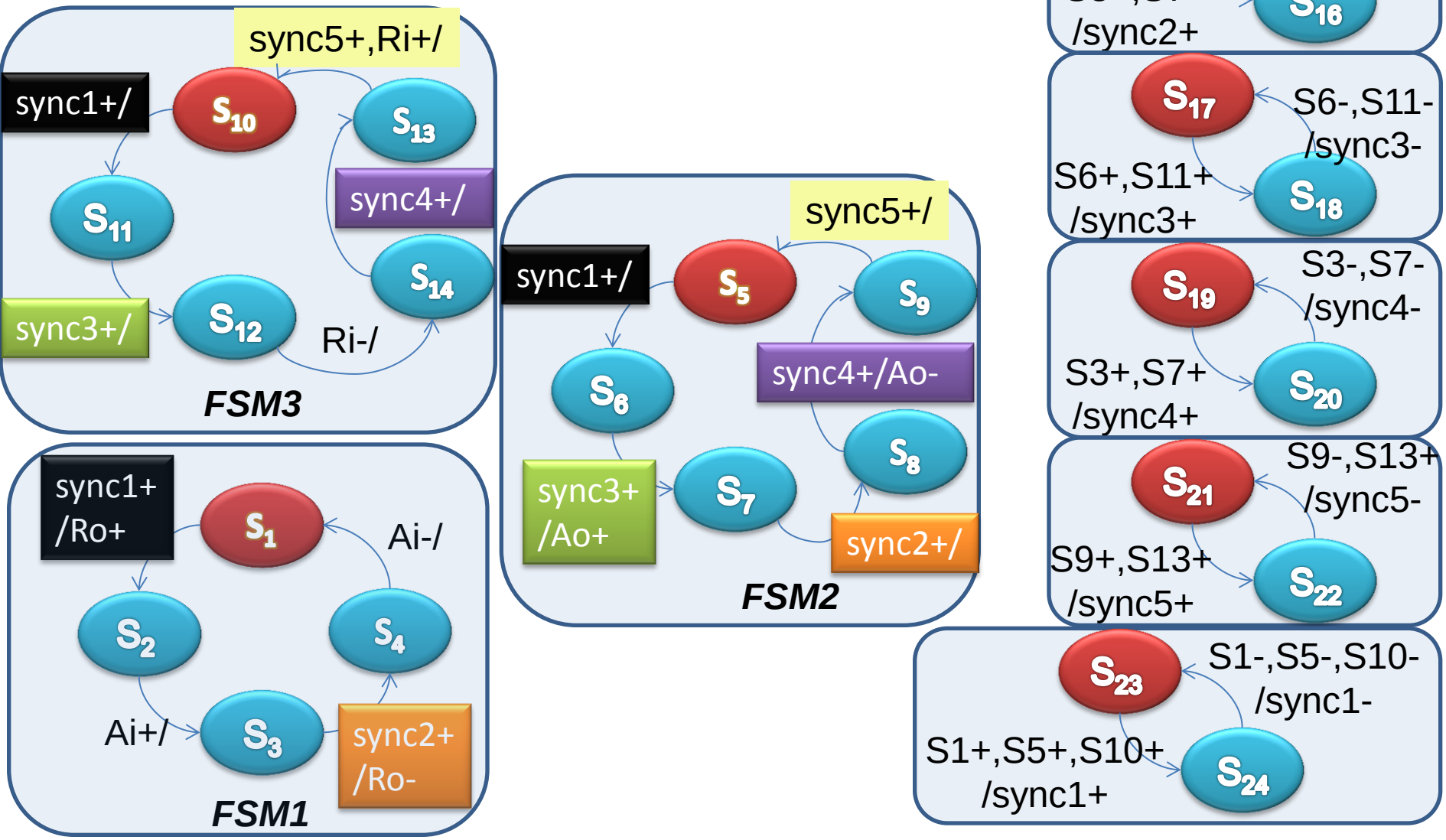
Synchronization Primitive Extraction

Synchronization Integration





Resultant Spec



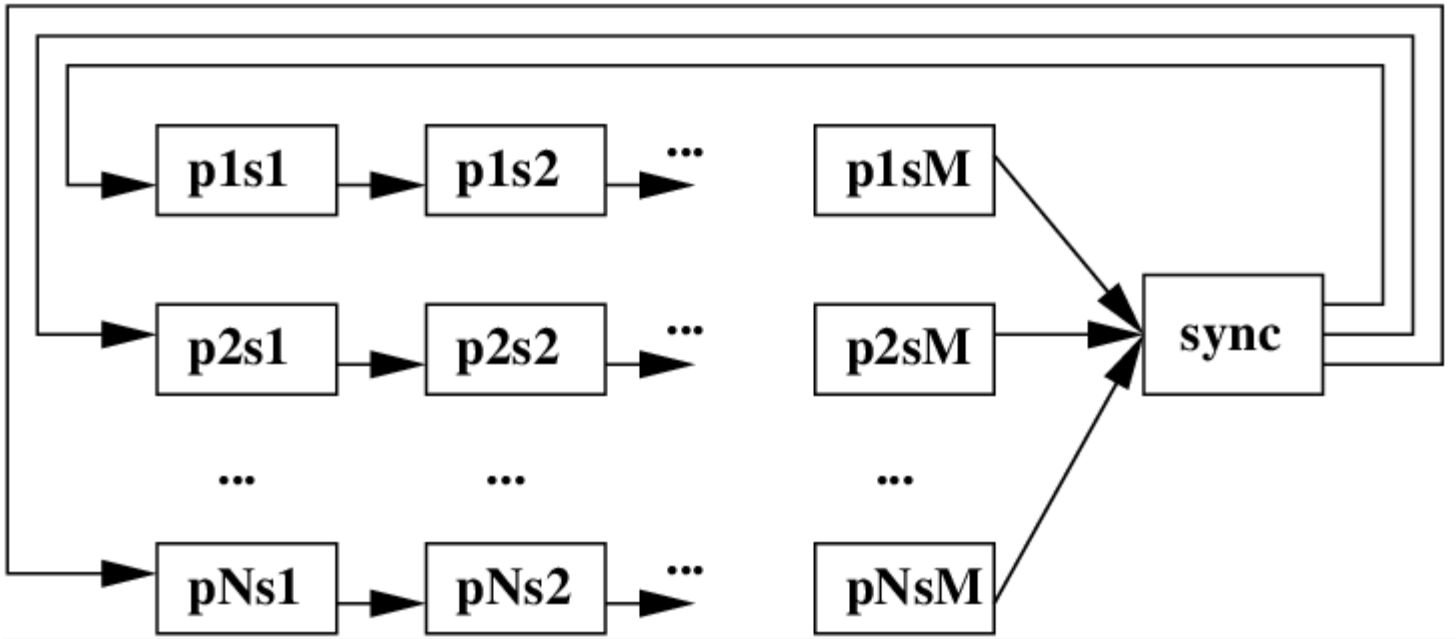
Complexity

$O(max(T^3P, P^2T^2))$	• Petrinet to S-Component Decomposition
$O(P^2T^2)$	• S-Component to BM-FSM Mapping
$O(P^3T^2)$	• Synchronization Primitive Extraction
$O(P^2T)$	• Synchronization Integration

Overview

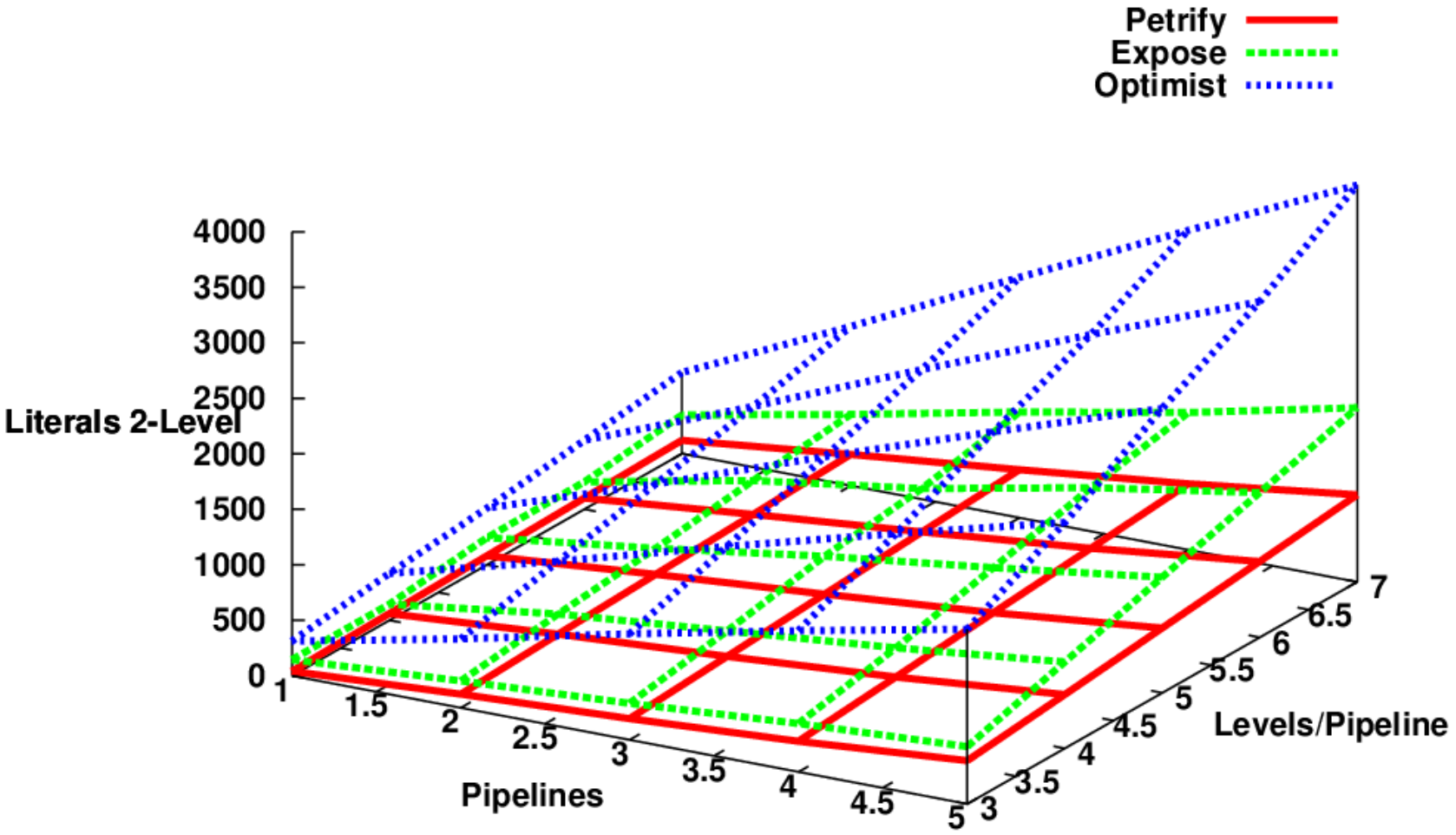
- Aim of this work
- Petrinet Operation
- Asynchronous Circuits Implementation Flows
- Proposed Flow
- ***Results***
- Conclusion and Future Work

Synthetic Benchmark

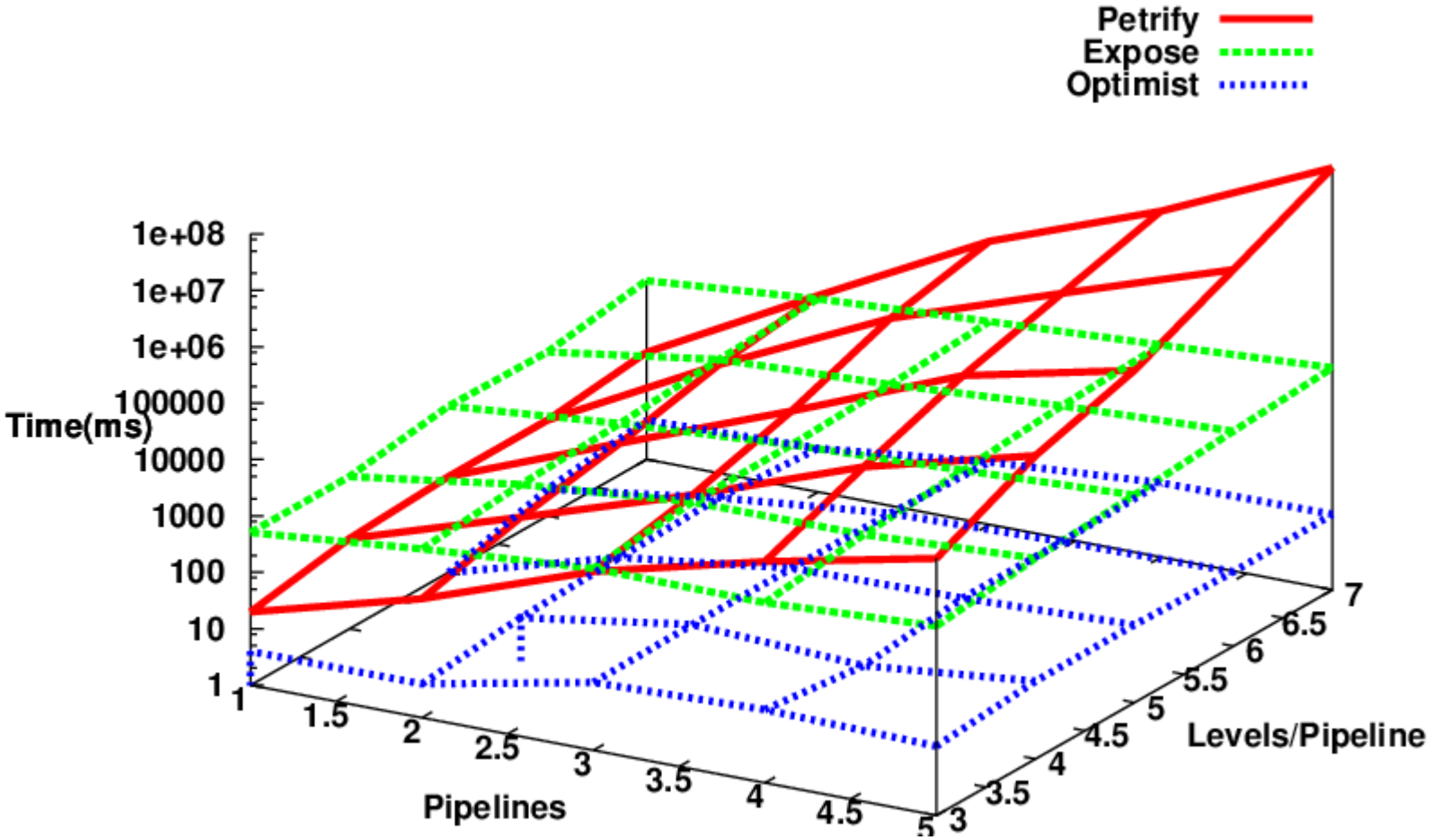


- N Parallel Handshake Controllers
- M Sequential Controllers Per Pipeline
- Synchronized at the M-th stage

Literal Count



Execution Time



Overview

- Aim of this work
- Petrinet Operation
- Asynchronous Circuits Implementation Flows
- Proposed Flow
- Results
- ***Conclusion and Future Work***

Conclusion and Future Work

- MSFSMs Used for Asynchronous Circuits Synthesis
- Introduced Expose Logic Synthesis Tool
  - Low Execution Time
  - High Quality Results
- Future Research Directions
  - Metric-Driven Synthesis of BM-FSMs
  - Examine BM-FSMs Operations
    - Composition/Decomposition