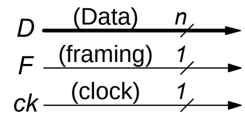
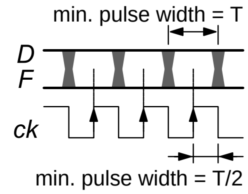
Parallel Transmission Links

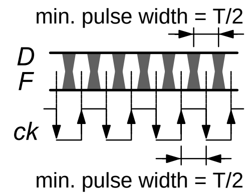


- Short distances (datapaths)
  - maintain synchronicity among wires
  - source-synchronous clocking (unidirectional) – partial-word clocking
- Framing
  - start-of-packet, end-of-packet
  - valid word – idle line
  - header delineation, etc.
  - *out-of-band* vs. *in-band* signaling
- Clocking (usually synchronous)
  - plain: clock wire signaling rate is twice other wires' signaling rate
  - DDR (double data rate): signaling rate is the same on all wires

Plain Clocking:



DDR Clocking:



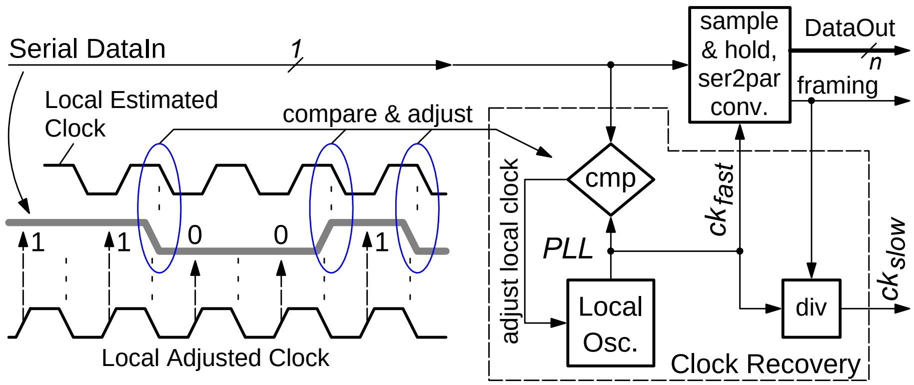
Parallel Link Forms / Concepts

Bit	Cell-Slice	Packet	Flow
bit 1 of 8 →	By. 1-8 →	packet 1 →	flow 1 →
bit 2 of 8 →	By. 9-16 →	packet 2 →	flow 2 →
bit 3 of 8 →	By. 17-24 →	packet 3 →	flow 3 →
bit 4 of 8 →	By. 25-32 →	packet 4 →	flow 4 →
bit 5 of 8 →	By. 33-40 →	packet 5 →	flow 5 →
bit 6 of 8 →	By. 41-48 →	packet 6 →	flow 6 →
bit 7 of 8 →	By. 49-56 →	packet 7 →	flow 7 →
bit 8 of 8 →	By. 57-64 →	packet 8 →	flow 8 →
	of 64B cell	*Inverse Multiplexing*	

same handling for all wires (same time, same destination) — Bit, Cell-Slice

different handling (diff. times & destinations) — Packet, Flow

Serial Transmission Links



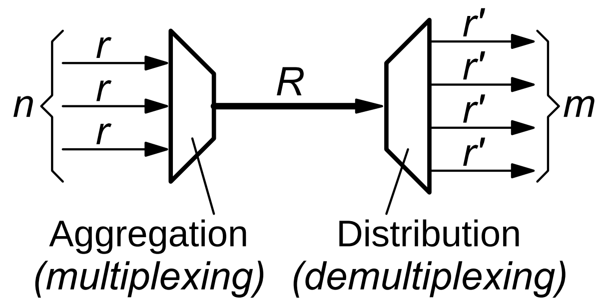
- Eliminate Timing Skew problem, Reduce Cost
- Clock Recovery from Data: phase-locked loop (PLL), need data to contain edges every so often ⇒ line coding, overhead (e.g. 8B/10B code)

Codes, Framing, Rate, Throughput, Capacity, Load

- Line Coding ⇒ extra *Control Characters* ⇒ framing
- Signaling Rate (*Baud* Rate): electrical “symbols” / second
  - binary digital transmission ⇒ 1 symbol = 1 bit
  - quadrature modulation ⇒ 1 symbol = 2 bits, etc.
- Transmission Rate: *raw* bits / second (raw *bps*)
- Throughput: *useful* bits / second (useful *bps*)

  Throughput = Transmission Rate *minus* Overhead
- Capacity: *peak* rate or throughput
- Load: current, actual (average) rate or throughput

Throughput Conservation



$$n \cdot r \;=\; R \;=\; m \cdot r'$$

- "instantaneous" (no buffering) or average (with buffering)
- what is conserved is the "useful-information" throughput
  - coding may change, idle bits added or removed, information may be filtered and/or selectively dropped, etc.

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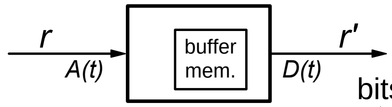
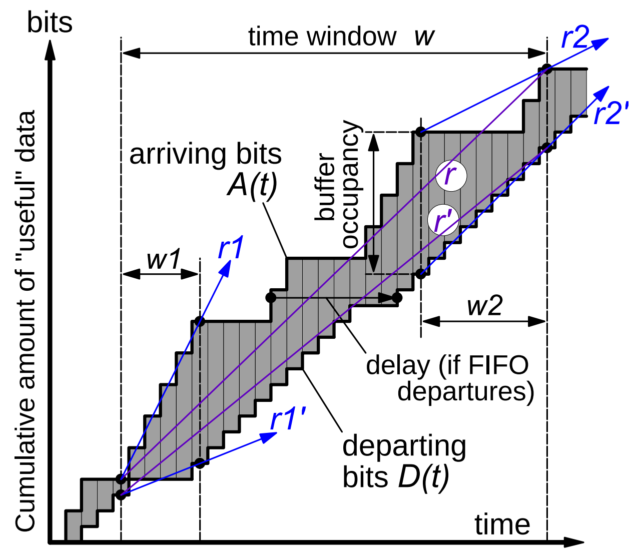


Buffer – Rate – Time Equation

$$B \geq |r - r'| \cdot w$$

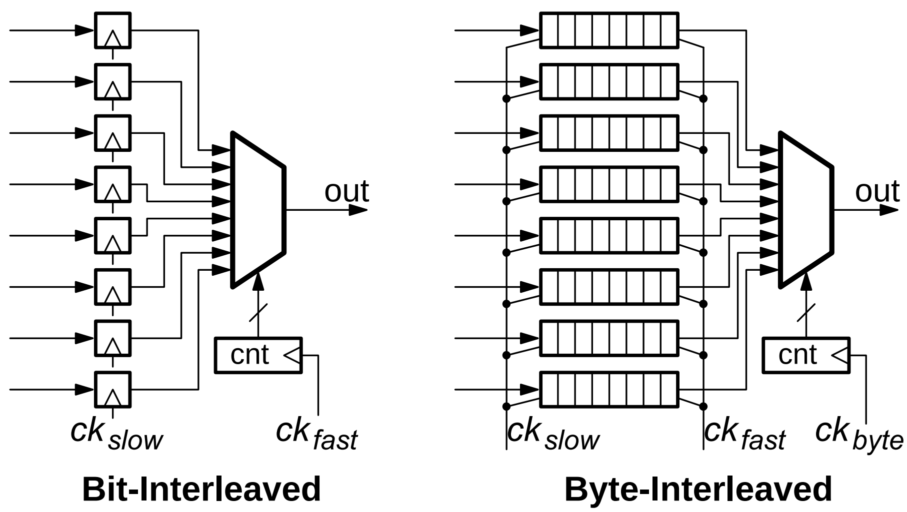


Buffer – Rate – Time Equation: Implications

$$B \geq |r - r'| \cdot w$$

- Throughput Conservation Law holds in the "long run"
- Time Scale for "long run" is proportional to Buffer Size
- Buffer is proportional to Burst Size
  - burst: a large rate difference that persists for a certain time window
- Average Delay = (Average Buffer Occupancy) / *r*
  - area between arrival – departure curves:
  - many vertical slices: (average buffer occupancy) · (time window)
  - many horizontal slices: (avg. delay) · (# of Bytes) = (delay) · *r* · *w* (assume FIFO departures, but same holds for non-FIFO)

Parallel-to-Serial Conversion: Multiplexing



Serial-to-Parallel Conversion: Demultiplexing