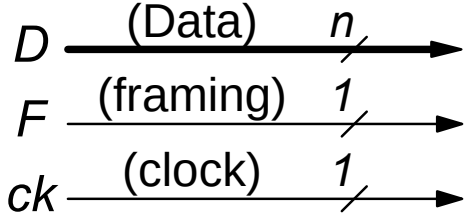
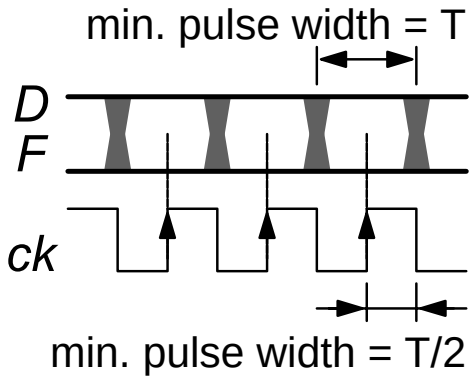
Parallel Transmission Links

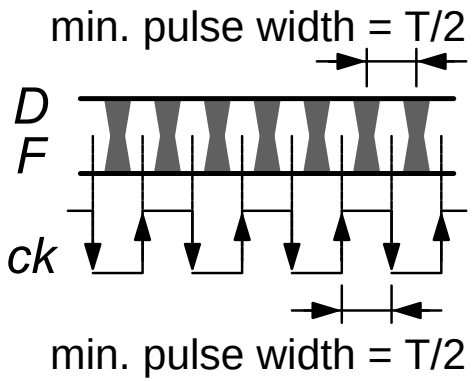
- Short distances (datapaths)
  - maintain synchronicity among wires
  - source-synchronous clocking (unidirectional) – partial-word clocking
- Framing
  - start-of-packet, end-of-packet
  - valid word – idle line
  - header delineation, etc.
  - *out-of-band* vs. *in-band* signaling
- Clocking (usually synchronous)
  - plain: clock wire signaling rate is twice other wires' signaling rate
  - DDR (double data rate): signaling rate is the same on all wires



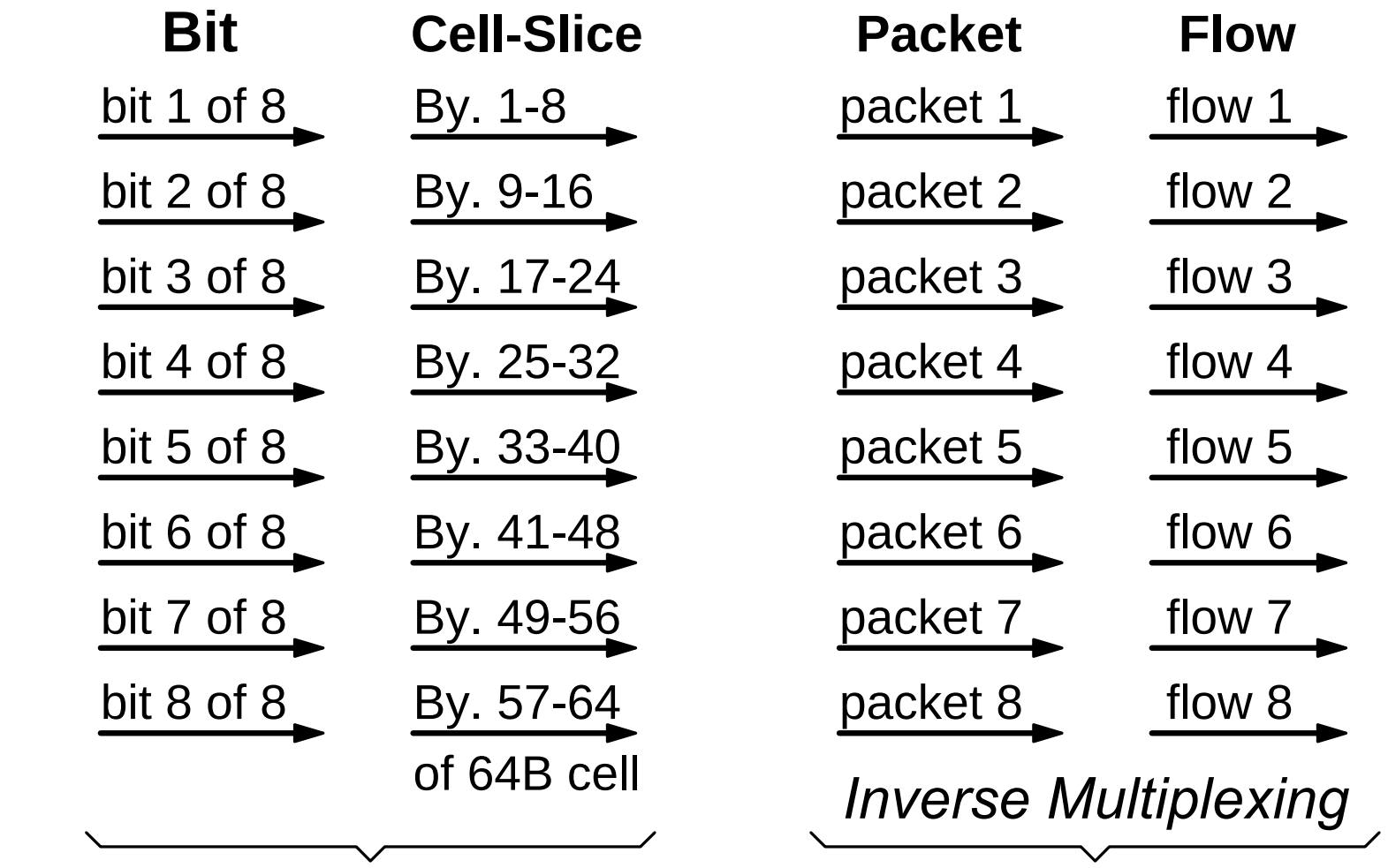
Plain Clocking:



DDR Clocking:



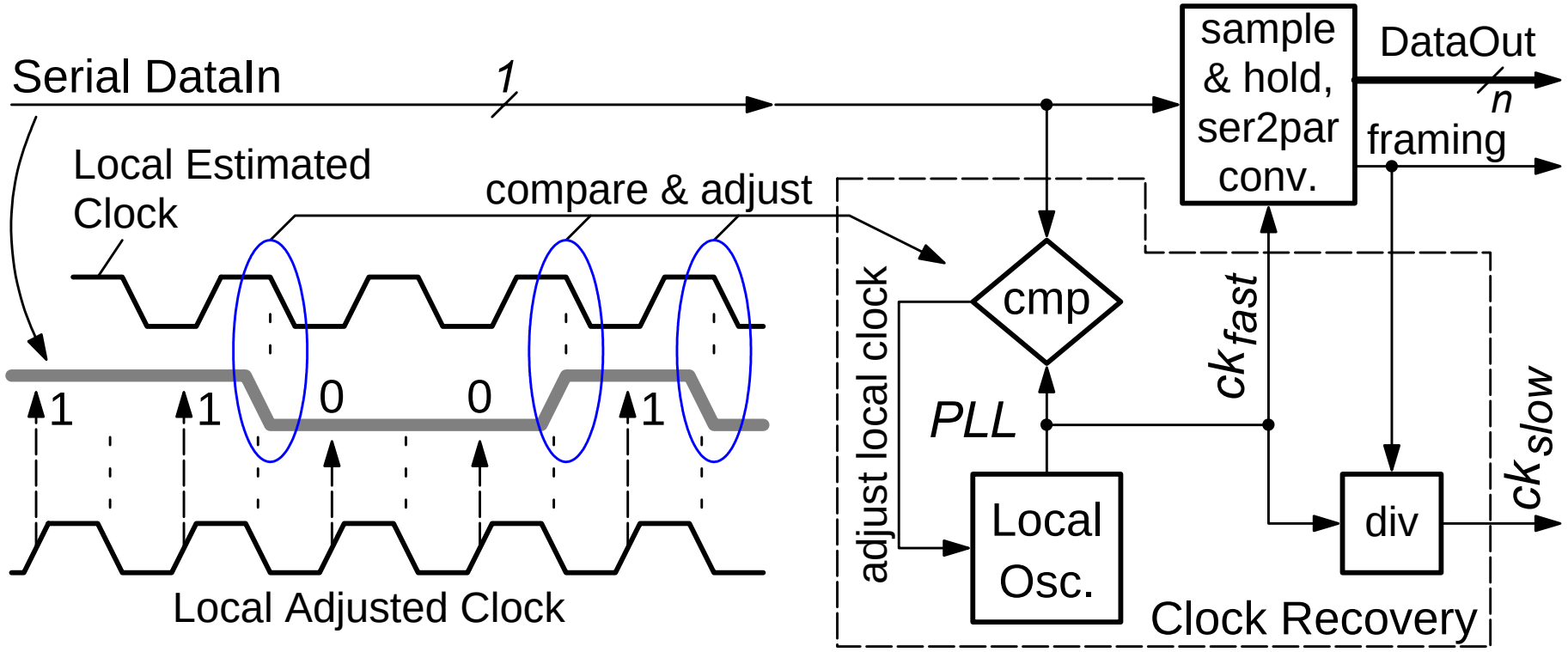
Parallel Link Forms / Concepts:



same handling for all wires
(same time, same destination)

different handling
(diff. times & destinations)

Serial Transmission Links



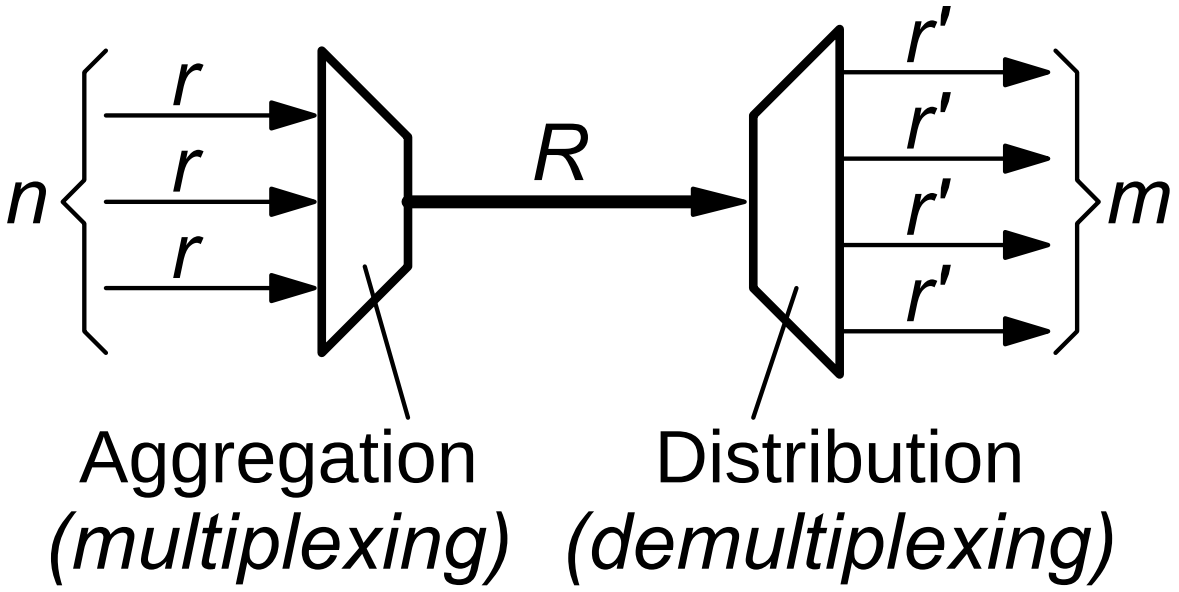
- Eliminate Timing Skew problem, Reduce Cost
- Clock Recovery from Data: phase-locked loop (PLL), need data to contain edges every so often ⇒ line coding, overhead (e.g. 8B/10B code)

Codes, Framing, Rate, Throughput, Capacity, Load

- Line Coding $\Rightarrow$ extra *Control Characters* $\Rightarrow$ framing
- Signaling Rate (*Baud* Rate): electrical "symbols" / second
  - binary digital transmission $\Rightarrow$ 1 symbol = 1 bit
  - quadrature modulation $\Rightarrow$ 1 symbol = 2 bits, etc.
- Transmission Rate: *raw* bits / second (raw *bps*)
- Throughput: *useful* bits / second (useful *bps*)

  Throughput = Transmission Rate *minus* Overhead
- Capacity: *peak* rate or throughput
- Load: current, actual (average) rate or throughput

Throughput Conservation



$$n \cdot r = R = m \cdot r'$$

- "instantaneous" (no buffering) or average (with buffering)
- what is conserved is the "useful-information" throughput
  - coding may change, idle bits added or removed, information may be filtered and/or selectively dropped, etc.

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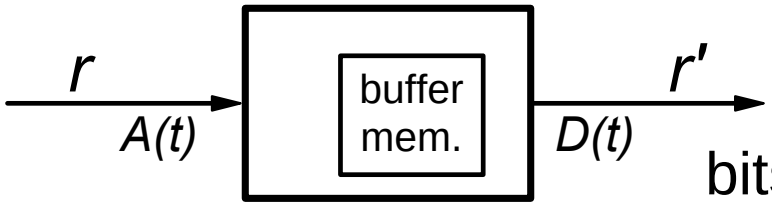
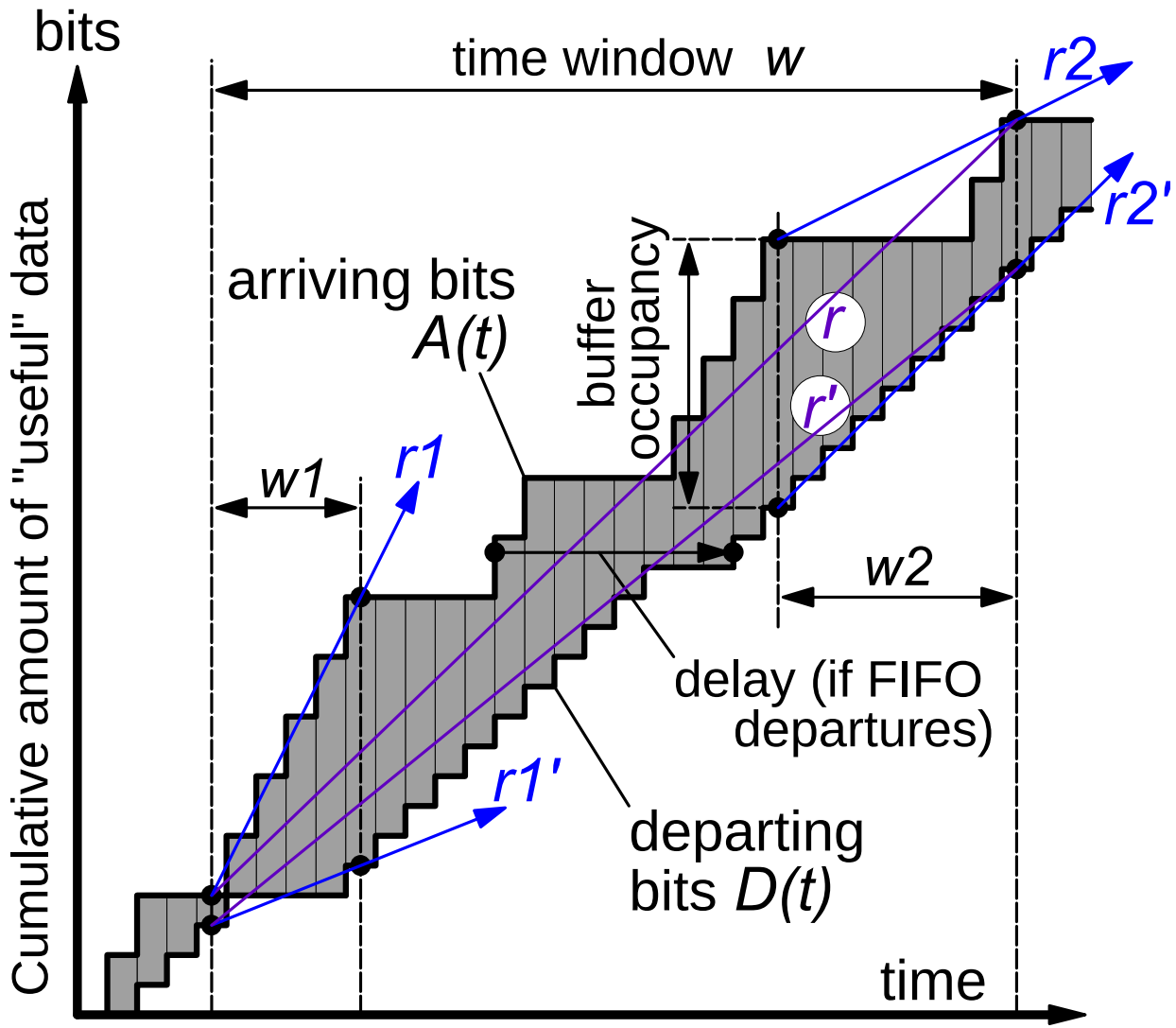


Buffer – Rate – Time Equation

$$B \geq \left| r\text{-}r' \right| \cdot w$$

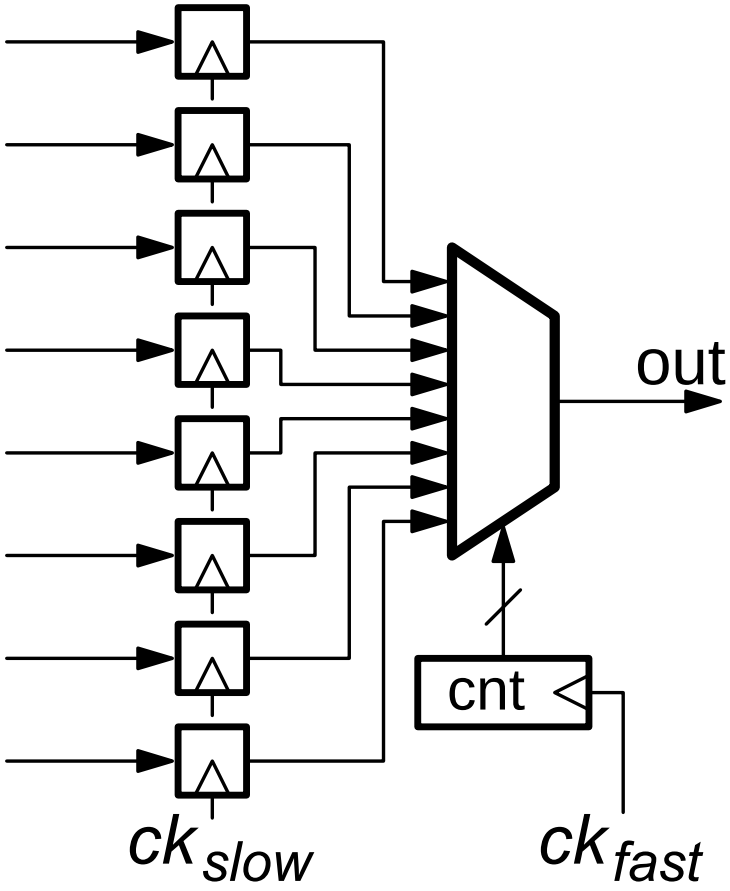


Buffer – Rate – Time Equation: Implications

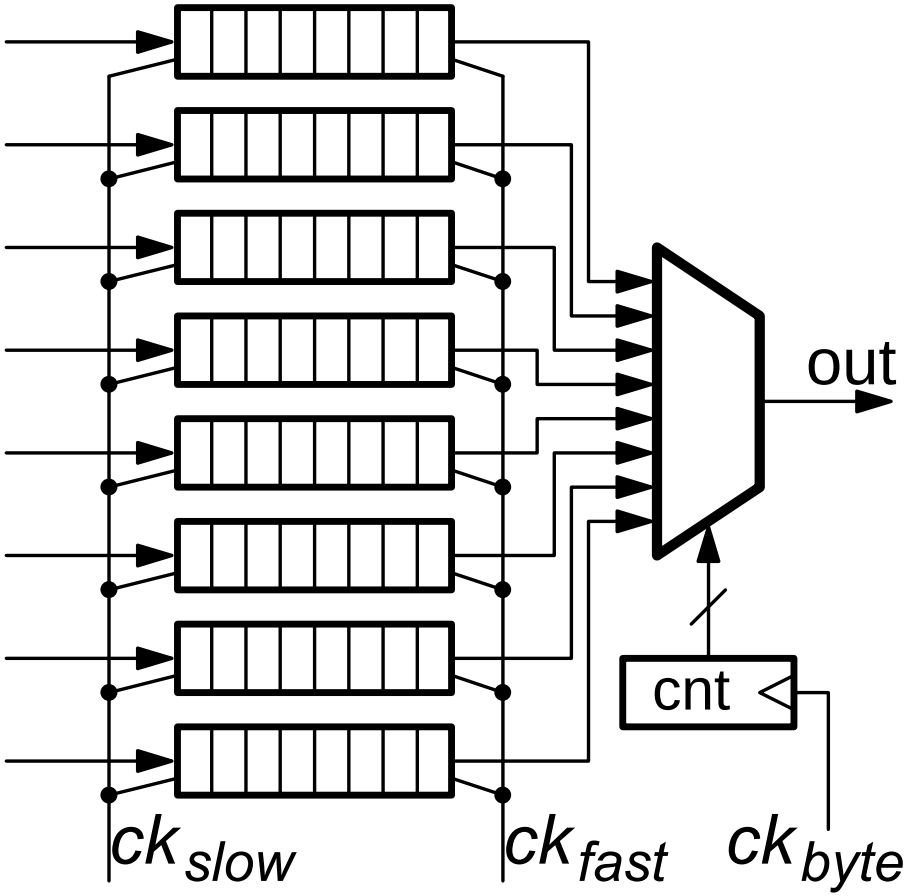
$$B \geq \left| r\text{-}r' \right| \cdot w$$

- Throughput Conservation Law holds in the “long run”
- Time Scale for “long run” is proportional to Buffer Size
- Buffer is proportional to Burst Size
  - burst: a large rate difference that persists for a certain time window
- Average Delay = (Average Buffer Occupancy) / r
  - area between arrival – departure curves:
  - many vertical slices: (average buffer occupancy) · (time window)
  - many horizontal slices: (avg. delay) · (# of Bytes) = (delay) · r · w
    (assume FIFO departures, but same holds for non-FIFO)

Parallel-to-Serial Conversion: Multiplexing

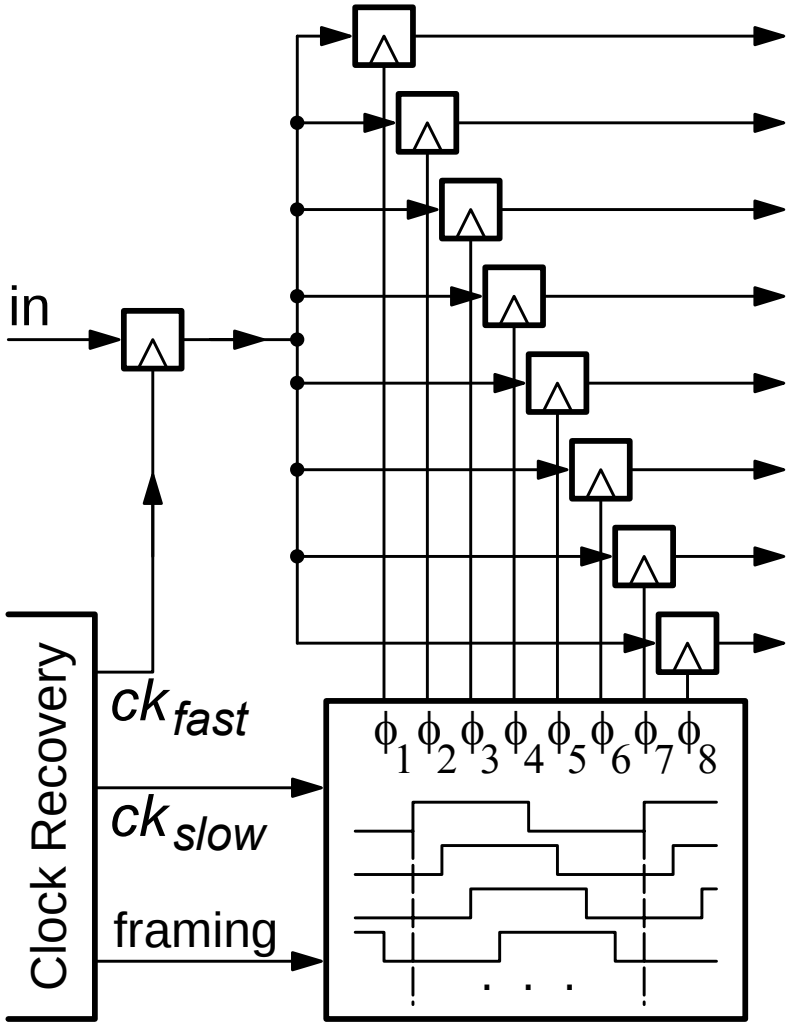


Bit-Interleaved

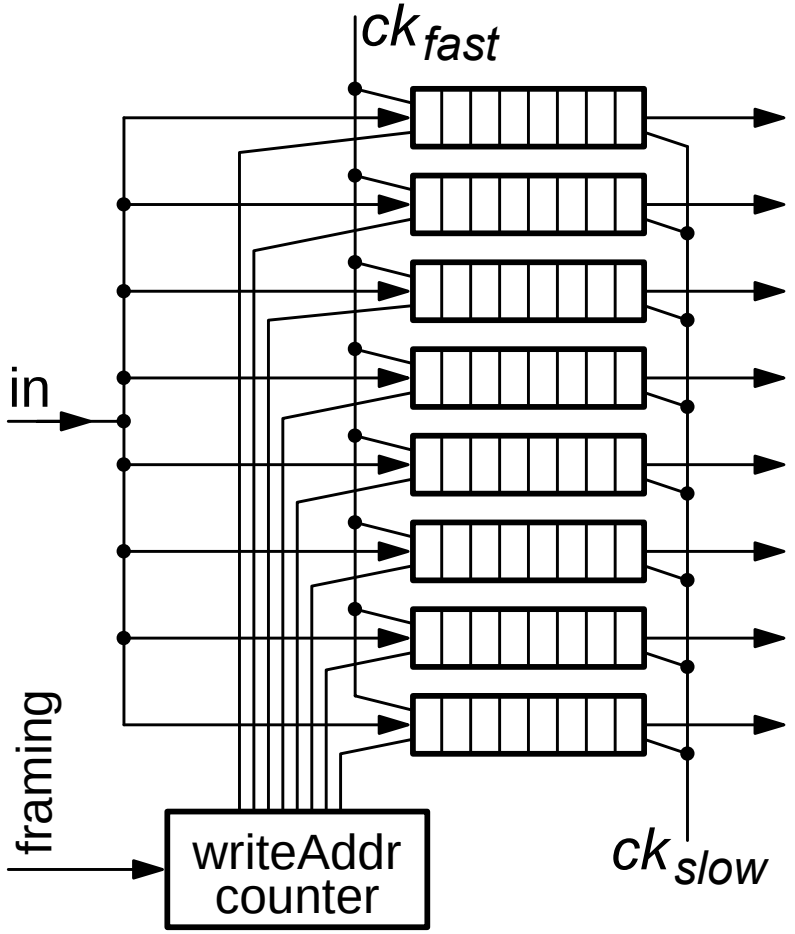


Byte-Interleaved

Serial-to-Parallel Conversion: Demultiplexing



Bit-Interleaved



Byte-Interleaved