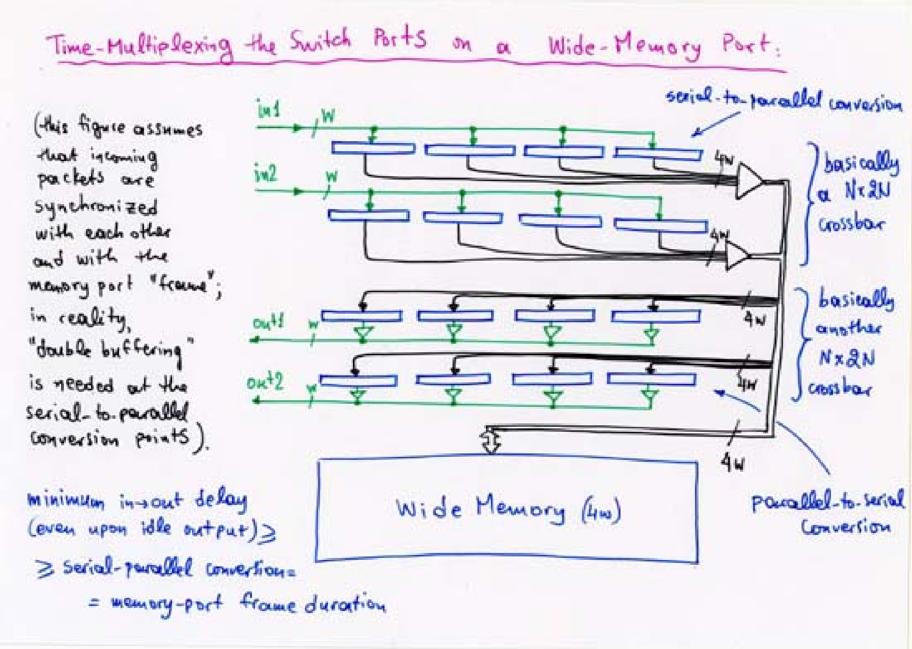
2.3 High-Throughput Memories for Time-Switching Shared Buffers

- Time-Switching applied to Packet Switching:
  - multiplex all incoming traffic onto a high-throughput internal shared path that leads into a *shared buffer*
  - read from the shared buffer and demux onto output ports
- High-Throughput Memories ⇒ Wide memories
  - how to best combine mux/demux and wide memory?
  - “pipelined memory”
  - interleaved memories & hidden crossbars

Time-Multiplexing the Switch Ports on a Wide-Memory Port:

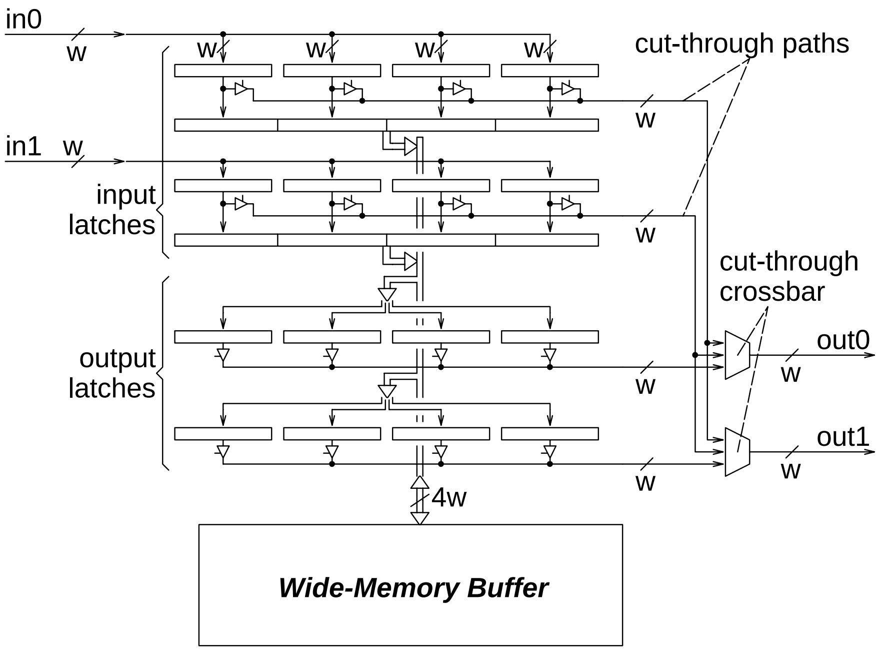

in1
W
in2
W
serial-to-parallel conversion
4W
4W
basically a Nx2N crossbar
out1
W
4W
out2
W
4W
basically another Nx2N crossbar
4W
Wide Memory (4w)
parallel-to-serial Conversion

(this figure assumes that incoming packets are synchronized with each other and with the memory port "frame"; in reality, "double buffering" is needed at the serial-to-parallel conversion points).

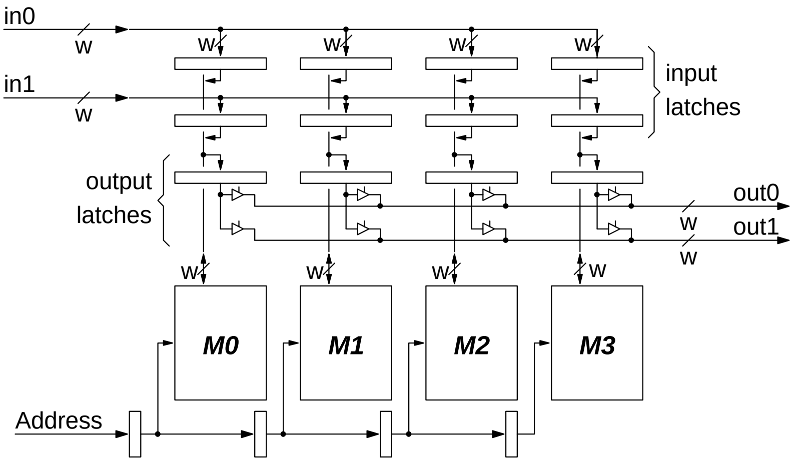
minimum in→out delay (even upon idle output) ≥

≥ serial-parallel conversion =

= memory-port frame duration



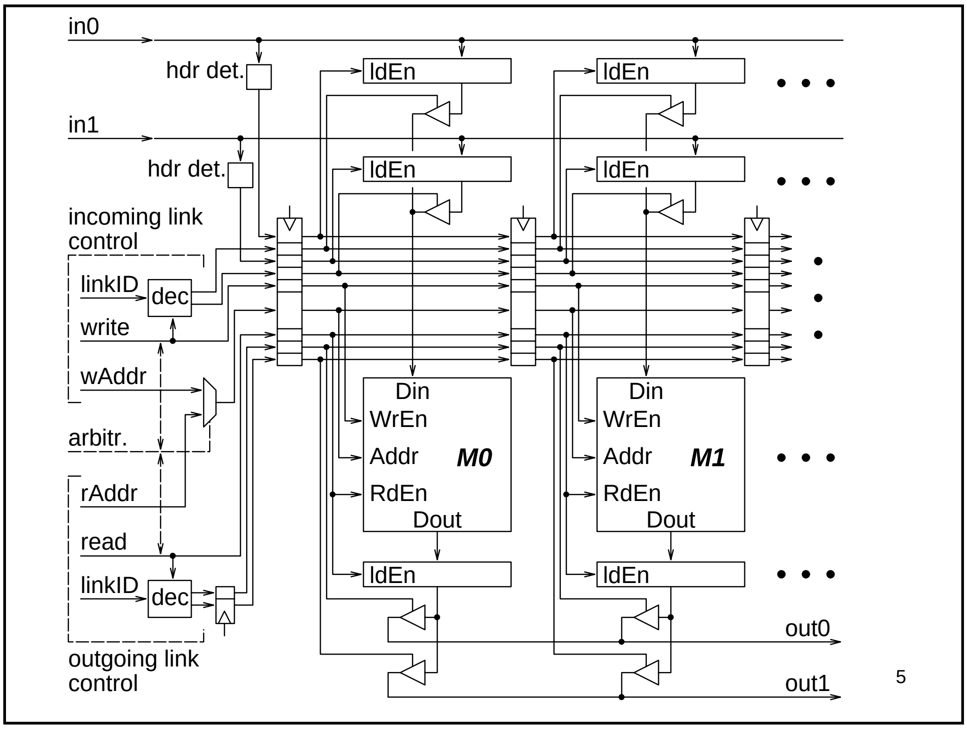
2x2 Shared-Buffer Switch using Pipelined Memor



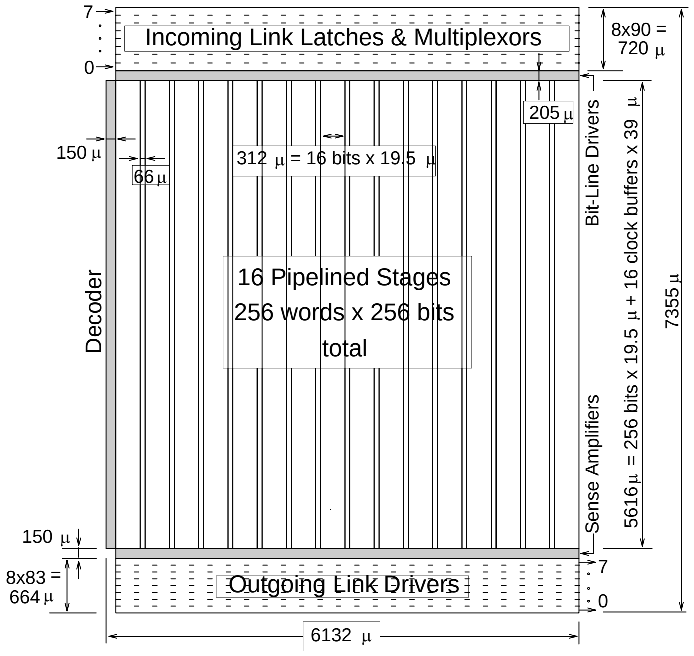
FORTH, Crete Greece (1994): USA Patent number 5,774,653 of 30 June 1998

Katevenis, Vatsolaki, Efthymiou: ACM SIGCOMM Conf., Sep. 1995. pp.39-48

`http://archvlsi.ics.forth.gr/sw_arch/pipeMem.html`



5



64 Kbit
Pipelined Memory
Shared Buffer
for an 8x8 Switch

1-micron
full-custom CMOS

Link throughput:
1.6 Gb/s (typical),
1.0 Gb/s (worst case)

ICS-FORTH,
Crete, Greece,
1995

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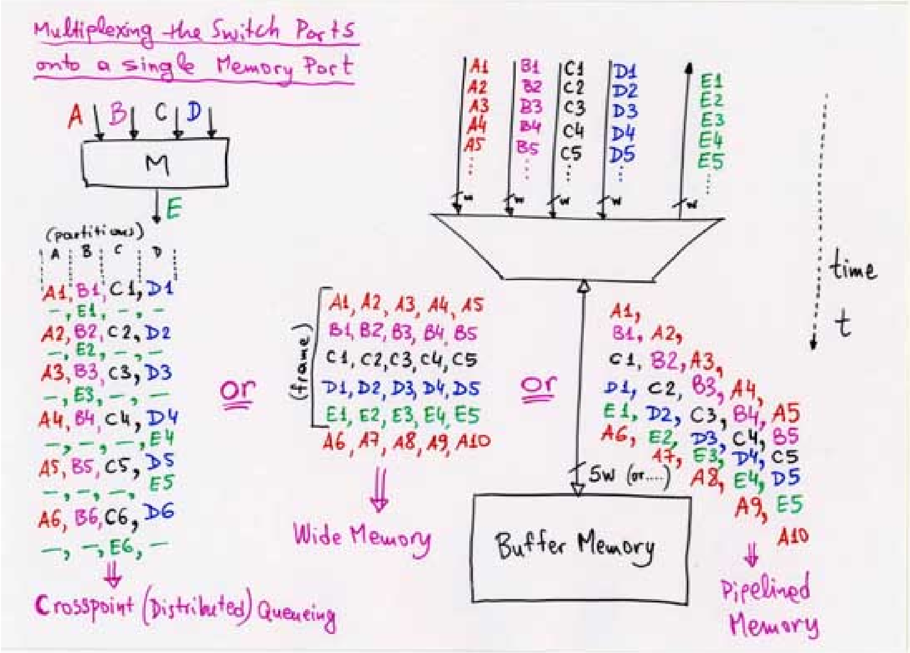
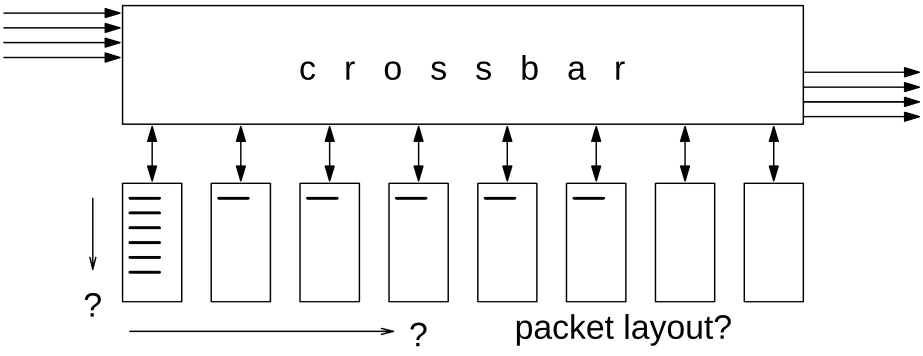
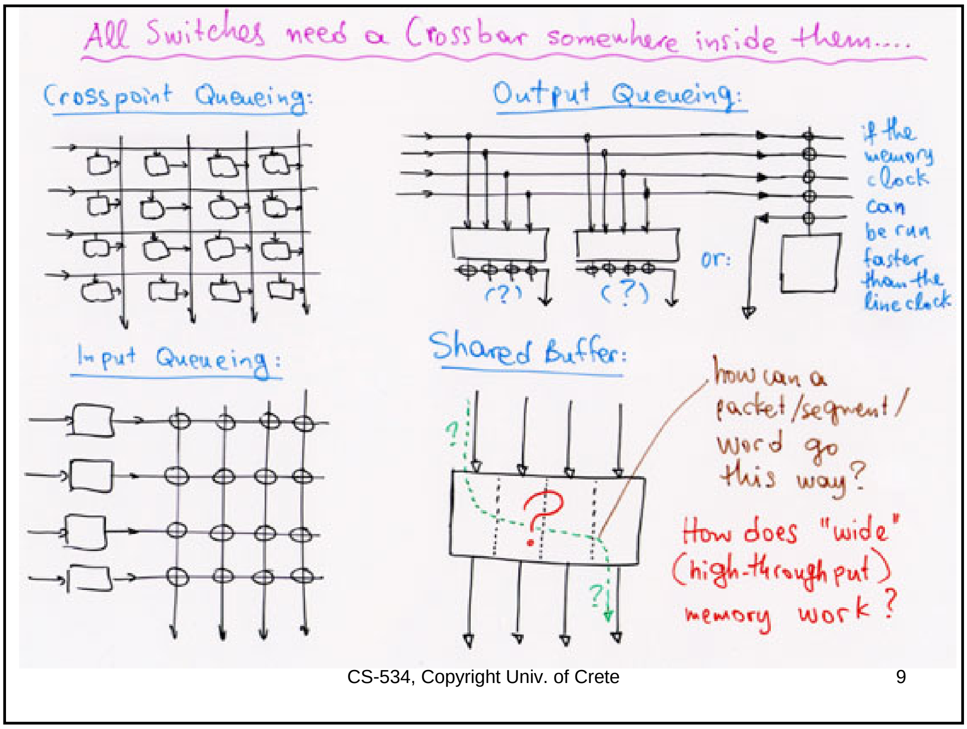
Multiplexing the Switch Ports onto a single Memory Port



High-Throughput Buffers: Interleaved Memories



- How to layout the packets so as to avoid bank conflicts?
- Is the memory so wide (number of banks so large) that some packets do not extend across all banks?



All Switches need a Crossbar somewhere inside them....

Crosspoint Queueing:

Output Queueing:

if the memory clock can be run faster than the line clock

Input Queueing:

Shared Buffer:

how can a packet/segment/word go this way?

How does "wide" (high-throughput) memory work?

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