2.2 Circuit Switching, Time-Division Multiplexing (TDM), Time Switching, Cut-through

- Circuit Switching versus Packet Switching
- Digital Telephony, Time-Division Multiplexing (TDM)
- Time Switching, Time-Slot Interchange (TSI)
- Switching and Computers: 1st and 2nd Generations
- Cut-through

Data are transmitted inside fixed, periodic frames; each circuit (connection) is allocated a fixed subset of the time-slots in each frame; connectionID and routing information is provided implicitly by the time-slotID in which a datum is transmitted.

The transmission capacity of a link is partitioned into a fixed number of circuits, each of them having a fixed rate; unused capacity in one circuit cannot be used by other circuits.

Advantage: simple.

Disadvantage: wasteful in transmission capacity, especially when actual rate of connections varies widely with time.
Multiplexing - Demultiplexing

at fixed aggregate capacity (circuit-switching style)

\[ CM = C_1 + \ldots + C_n \]

Examples:
- circuit switching: frames & time-slots
- wide (bit-parallel) buses inside switch elements

Minimal buffering requirements:
- one time-slot-worth of data per mux'ed/demux'ed link

Partitioned versus Shared Link Capacity

Resource Partitioning leads to Underutilization:

In a link carrying multiplexed traffic of fixed aggregate capacity type, the flows in one partition may lack capacity, while other partitions may have excess capacity. This is the disadvantage of circuit switching.
Packet Switching

- Non-periodic multiplexing of packets, on a demand basis; each packet carries its own source and destination (connection) ID, and can be stored and forwarded at any later time.
- The transmission capacity of a link is shared among all flows (connections) that pass through it, on a demand basis; any capacity that is not used by one flow can be used by another.
- Advantage: no waste of transmission capacity.
- Challenges:
  - dynamic control (per packet), rather than static (at conn. set-up);
  - unpredictability of traffic, leading to contention for resources.

Packet Switching: Statistical Multiplexing

\[ C_1 + ... + C_n = C_M > C_m \]

- Fixed aggregate capacity multiplexing (circuit switching)
- Not fully utilized all the time
- Partitioned capacity
- Buffer required to absorb transients when \( \lambda(t) > C_m \)
- Shared capacity (packet switching)
Digital Telephony

- Telephone quality voice ≤ 3.5 kHz → ≈ 8000 samples/second
- 2000 samples/s x 8 bits/sample = 16,000 bits/s → one digital telephony circuit

Time-Division Switching

- Frame structure with data and address
- Connection table with connection
- Time-Slot Interchange (TSI)
Time-Division Switching:

When each external link carries a single connection, the time-slot interchange can be merged with the multiplexer (or with...

Note: for switching to be possible, it is essential to have a single, shared link going from all inputs to all outputs. Every single quantum of information goes through that single common link. The throughput of that link = \( \Sigma \) input = \( \Sigma \) output. In this case, \( \text{fast clock} = n \cdot \text{slow clock} \) (no extra lines).
Time-Division Switching: more complex case:
- Many connections per external line
- Different bit rates for different channels
- Internal TSI needed with full frame of bit-serial data
- Internal TSI cannot be merged with mux or demux
- Worst-case delay = 1 frame time, again.

A1, A2, A3 are arranged such that input signals arrive in correct time slot. However, not so for A8, A9, as both input signals arrive on same link. Cannot be placed both in correct time slot.

Discussion: Can I freely rearrange positions of connections inside input and output frames?

---

Byte-by-Byte Time Switching: Throughput Limit?

Write address → TSI Data Mem. → Read address

Assume 300 MHz 2-port SRAM

Peak Throughput = \( \frac{300 \text{ MHz}}{3} = 100 \text{ Gbps} \)

Can we increase throughput by widening the TSI memory?

128 bits = 16 bytes

16 bytes x 300 MHz = 48.4 Gbps/s

What is the multiplexing quantum??

- 16 bytes belonging to a same 64 Kbps channel:
  - must wait 16 frames = 16 x 125 μs = 2 ms to collect all these bytes.
  - buffer size for collection = 2 ms x 38.4 Gbps = 76.8 Mbytes

- 16 bytes belonging to 16 "adjacent" 64 Kbps channels:
  - must switch all 16 channels together:
    where one of them goes, all 16 of them must go!
Time Division Switching:
From Circuit Switching to Packet Switching

...from statically, off-line scheduled, fixed-throughput/ channel to dynamically, demand-driven, online scheduled, variable-throughput/word or block transactions

**Issues:**
- Granularity of transfers in input, Mean/Out (multiplexing quantum):
  - Fine grain... (narrow mem/blk)
  - Small buffers in I/O
- Narrow mem → small throughput
- Small packets OK!
- Access rate/blk more important

- Control structure & operation:
  - Where to store words or blocks of each packet? scattered?
  - Can I mix multiple packets in one block?
  - Where to store the packets going to a certain output link?
  - (or from a certain input link?) (or of a same QoS class?)

"First Generation" Switches

- CPU
- Memory
- Shared bus
- Line cards
  - Typically, in 2 out on same card
- w/o DMA: each packet bit 4 times through the bus
- w/ DMA: each packet bit twice through the bus
Cut-through reduces delay. Hiccup-less cut-through requires:

- hiccup-less incoming packets
- controlled rate difference between input and output