

HY425 - Αρχιτεκτονική Γεωλογιστών

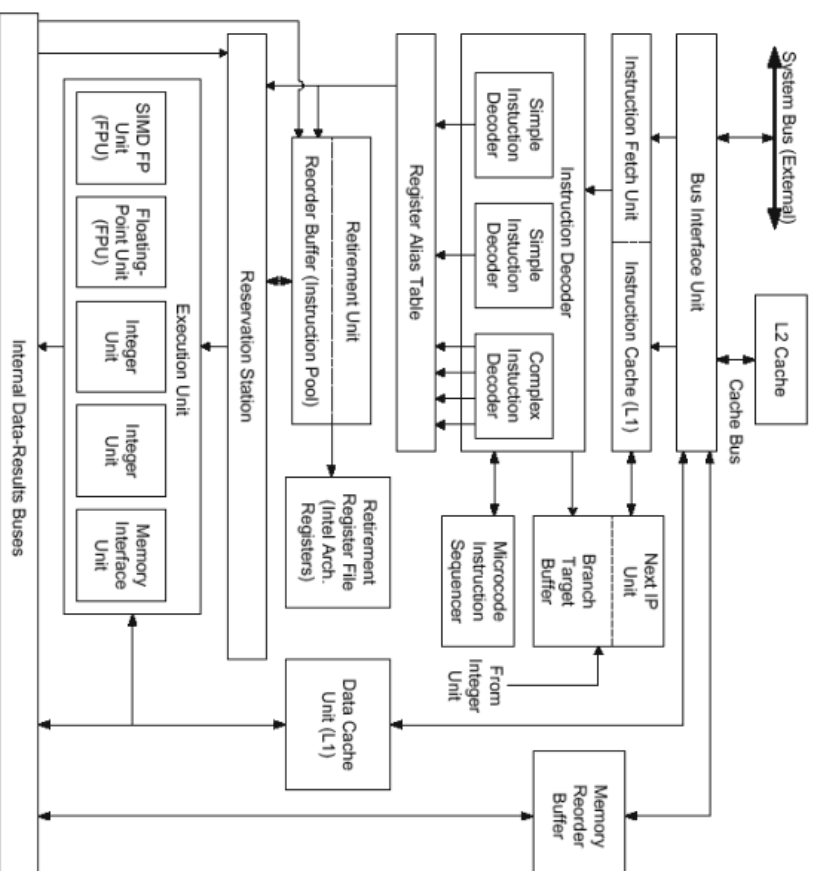
Χ. Σωτηρίου

21 Οκτωβρίου 2001

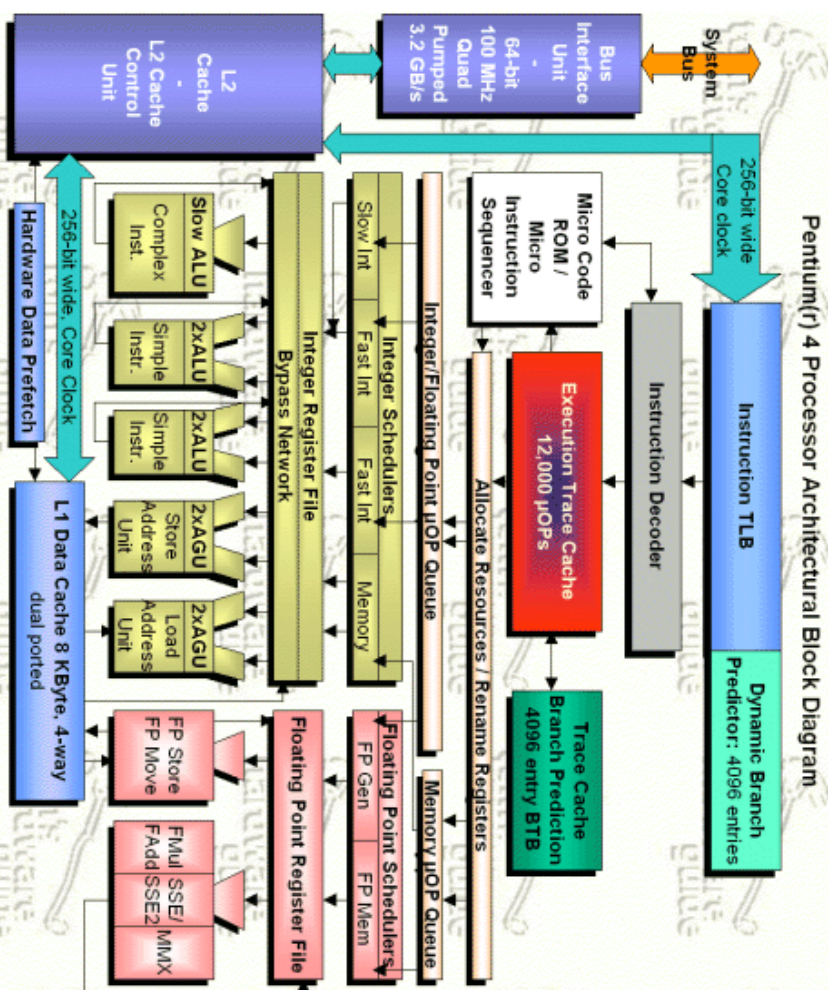
Ιστορία της Αρχιτεκτονικής 80x86

Επεξεργαστής	Ημ. Έκδ.	Συχν.	Αρ. Τρανζ.	Κατ.	Bus Δεδ.	Διευθύνσεις	Cache
8086	1978	8MHz	29K	16-bit GP	16	1MByte	-
80286	1982	12,5MHz	134K	16-bit GP	16	16MBytes	-
80386DX	1985	20MHz	275K	32-bit GP	32	4GBytes	-
80486DX	1989	25MHz	1,2M	32-bit GP, 80-bit FP	32	4GBytes	8KBytes L1
<i>Pentium</i>	1993	60MHz	3,1M	32-bit GP, 80-bit FP	64	4GBytes	16KBytes L1
<i>Pentium Pro</i>	1995	150MHz	5,5M	32-bit GP, 80-bit FP	64	64GBytes	16KBytes L1 256, 516, 1M L2
<i>Pentium II</i>	1997	266MHz	7M	32-bit GP, 80-bit FP, 64-bit MMX	64	64GBytes	32KBytes L1 256, 516 L2
<i>Pentium III</i>	1999	500MHz	8,2M	32-bit GP, 80-bit FP, 64-bit MMX, 128-bit XMM,	64	64GBytes	32KBytes L1 256, 516 L2

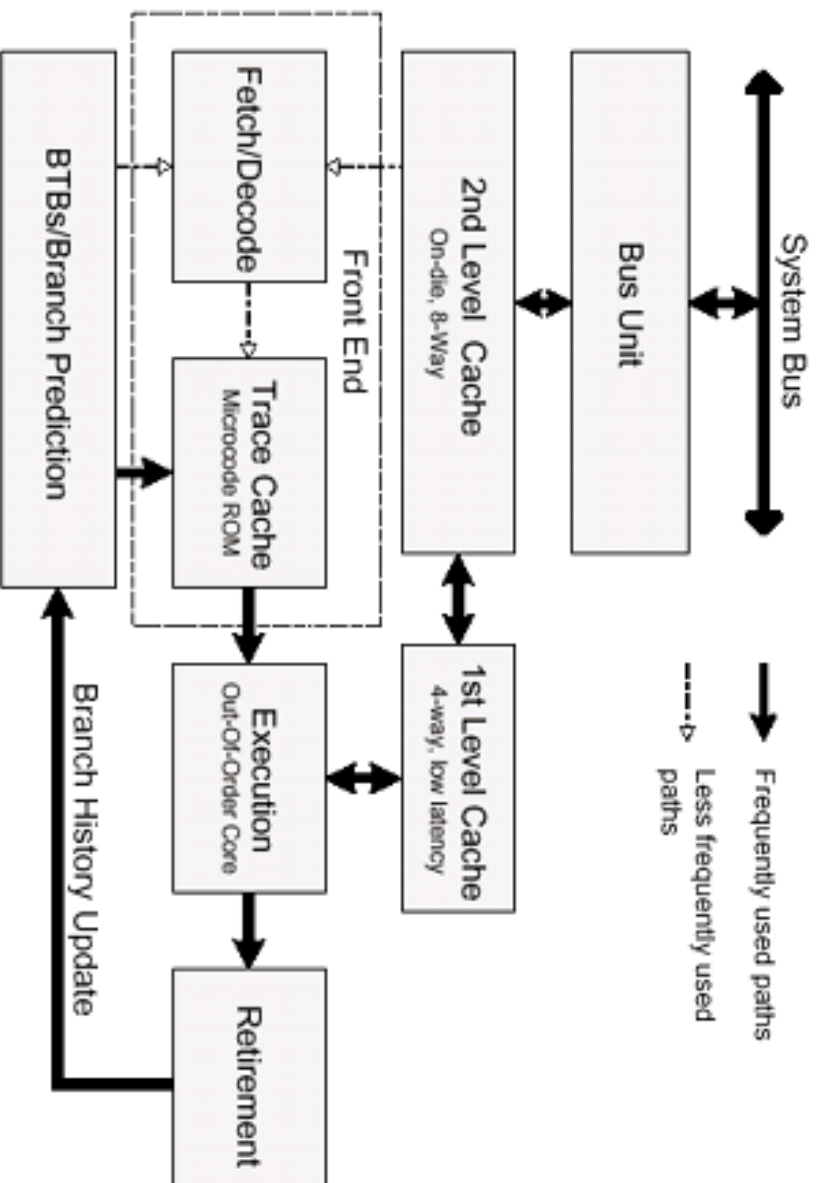
Αρχιτεκτονική P6 - Pentium III



Αρχιτεκτονική *Pentium4*



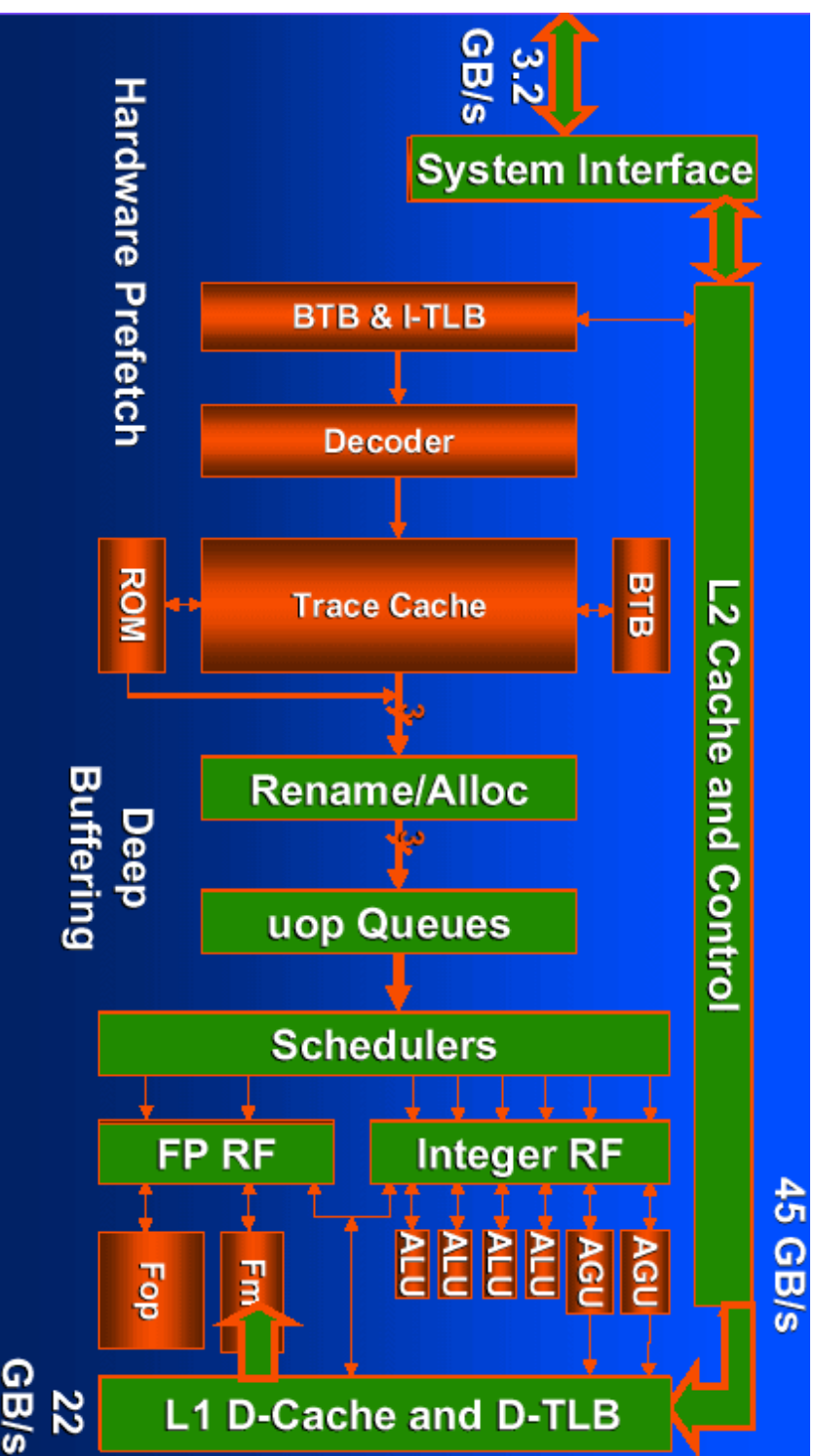
Αρχιτεκτονική *Pentium4*



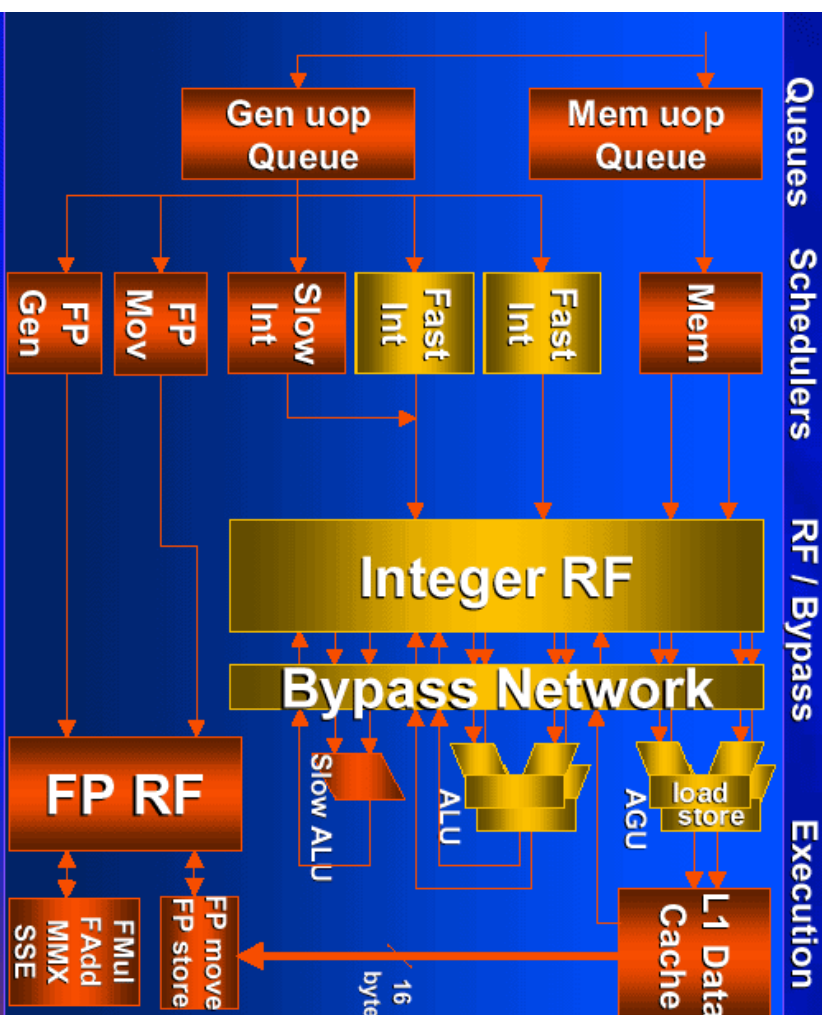
Κλιμάκωση *Pentium4* - 20 Στάδια*Neburst?*

1	2	3	4	5	6	7	8	9	10
TC	Nxt IP	TC	Fetch	Drive	Alloc	Rename	Que	Sch	
11	12	13	14	15	16	17	18	19	20
Sch	Sch	Disp	Disp	RF	RF	Ex	Flgs	Br Ck	Drive

Κλιμάκωση *Pentium4*



Κλιμάκωση Pentium4 - RFE



Pentium4 - Trace Cache

The screenshot displays a trace cache with three entries, T1, T2, and T3, each containing a sequence of instructions. The instructions are color-coded: green for 'cmp', red for 'br', and blue for other instructions. Red arrows indicate branch targets.

T1:	1 cmp	2 br -> T1	3 T1: sub
	... (unused code)		
T2:	1 sub	2 br -> T2	3 T2: mov
	... (unused code)		
T3:	1 add	2 br -> T3	3 T3: mul
	... (unused code)		

Pentium4

