DIGITAL CAMERA SYSTEM ON A CHIP

ORIGINALLY DESIGNED FOR NASA, CMOS-TECHNOLOGY DIGITAL CAMERA SYSTEMS ON A CHIP HOLD GREAT COMMERCIAL APPLICATION POTENTIAL.

Eric R. Fossum
Photobit Corporation

Since the early 1990s, an explosion of activity in the area of CMOS image sensors has taken place. Up until recently, the dominant, and nearly the only, solid-state image sensor technology was the charge-coupled device (CCD). However, most microprocessors, logic circuits, ASICs, and memory circuits are based on CMOS technology. Now CMOS can be used for image sensors in a rapidly expanding sphere of applications.

Several important factors have contributed to the emergence of CMOS image sensors at this time rather than 10 to 20 years ago. The primary factor consists of recent demand for portable, low-power, miniaturized digital imaging systems. A second important factor is that present-day CMOS offers submicron feature sizes and low defect and contamination levels, permitting cost-effective pixel sizes and low junction leakage (or *dark*) current.

In addition, threshold voltage control and uniformity is stable and reproducible. The third important factor, new circuit techniques that have been invented or adopted from CCD signal processing, permits both low noise and high dynamic-range imaging that is competitive with the best CCDs. This includes the development of active pixel sensor technology and column-parallel, signal-processing circuits for temporal and fixed-pattern noise reduction.

Using technology originally developed at NASA Jet Propulsion Laboratory, we formed Photobit to further develop and commercialize CMOS-technology systems on a chip. The digital camera on a chip has applications not only in aerospace but also in a large array of commercial products like cameras.

To get a better handle on digital camera systems on a chip, let's review CMOS image sensor technology basics, look at the state of the art, and try to determine where the technology may be leading us.

Imaging systems

Figure 1 shows an overall view of an imaging system. Optics collect and focus photons reflected off an object onto an array of photodetectors or pixels. The photodetectors convert the photons into a charge that is integrated over a period, perhaps 33 milliseconds (corresponding to a 30-Hz frame rate). At the end of the integration period, the array of accumulated charges must be read out, processed, and converted into a video signal. In a digital camera on a chip, all electronics reside on a single chip, and all electronic input signals as well as the output video stream are digital.

Pixels implemented in silicon have an intrinsically panchromatic response to visible and near-infrared (NIR) photons. Wavelength dependent, the quantum efficiency (QE) of the pixel is the ratio of electrons (or holes) col-

0272-1732/98/$10.00 © 1998 IEEE

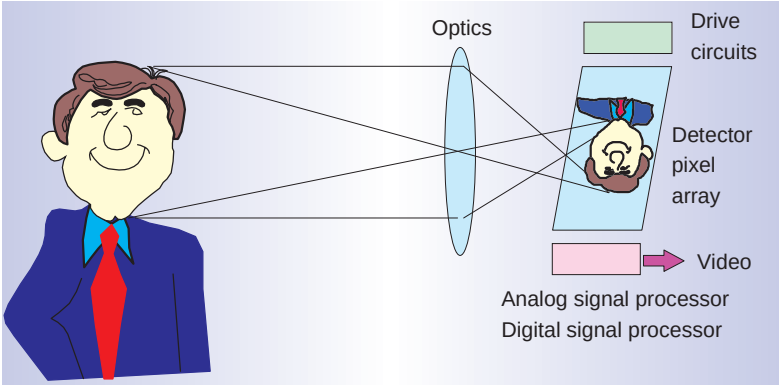

Figure 1. Imaging systems include not only pixel arrays but also optics, drive electronics, and analog and digital processing electronics.

Glossary

ADC	analog-to-digital converter
ASP	analog signal processor
APS	active pixel sensor
CCD	charge-coupled device
CDS	correlated double sampling
CFA	color filter array
CMOS	complementary metal-oxide semiconductor
FIT	frame interline transfer
FPN	fixed-pattern noise
FT	frame transfer
ILT	interline transfer
JPL	Jet Propulsion Laboratory
NIR	near infrared
PPS	passive pixel sensors
QE	quantum efficiency

lected to incident photons. Each photon generates either one or zero electrons in the silicon, each of which may or may not be collected by the pixel. The average QE across a pixel typically equals 30% in the visible range. For most applications, matching the response of the sensor to that of the human eye simplifies the rendering of a color image. A NIR cutoff filter inserted in the optical system often eliminates the effect of NIR photons on the collected signal.

To generate a color image, each pixel is covered with a separate filter. Both red (R), green (G), blue (B) color and complementary cyan (C), magenta (M), yellow (Y) color space patterns are used, though RGB systems are more common. The filters laid on top of the pixels (see Figure 2) form a pattern that enables RGB reconstruction at each pixel (through subsequent interpolation by signal processing). Maximum spatial resolution is typically sought for the green channel, again to match the human eye.[1]

In addition to the deposition of a color filter array (CFA) pattern, microlenses are also used. This is because pixels often divide into two portions—a portion sensitive to light and a portion for readout that is typically insensitive to light. The ratio of the sensitive region to the total pixel area (called the fill factor) is typically designed to be about 25% to 30%, though higher is better.

The use of a microlens helps concentrate light that would normally be incident on the insensitive readout portion of the pixel to the sensitive portion of the pixel.[2] The microlens is implemented either using a polymer-thin film or by etching the glass deposited on the chip. Microlenses typically improve the effective fill factor in image sensors by about 2 to 3 times (up to 75% to 80%).

CCDs—a background

CCDs, the first generation of solid-state image sensors, have evolved to a high level of performance over the 28 years since their invention. CCDs and CMOS image sensors are both implemented in silicon. Silicon properties dictate image sensor wavelength response and the sensor's ultimate sensitivity. Fundamentally, CCDs and CMOS image sensors can have identical responses to light, since both depend on the absorption of light by silicon and the collection of photogenerated electrons (or holes). It is in the readout of

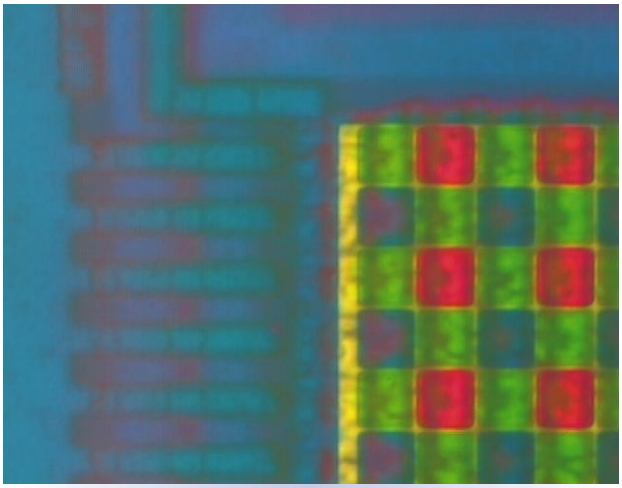

Figure 2. Corner of CMOS active pixel sensor (APS) with RGB color filter array (CFA) deposited on pixels. Pixel size is 7.9×7.9 μm.

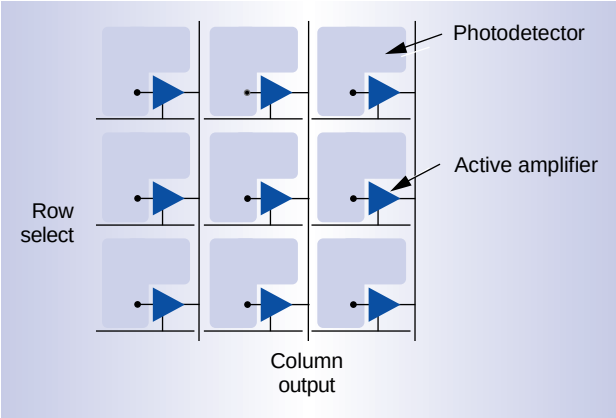

Figure 3. Active pixel sensors have an amplifier built into every pixel for lower noise and faster readout.

these signals that the similarity ends.

The CCD uses a charge-coupling technique to shift collected electrons out to an output amplifier. The efficient shifting of electrons through thousands of stages requires a CCD fabrication process that is different in recipe from mainstream microelectronics, and relatively high operating voltages to pull the electrons along from one stage to the next. The charge is shifted to a single analog output amplifier located at the corner of the array, and the output of the CCD is an analog video signal. The shifting action of the CCD can result in image blurring if the charge is not shifted under a light shield, and even then it is subject to smear from the collection of carriers despite the light shield.

Three approaches to rapidly moving the charge under a light shield exist. The first, frame transfer (FT), shifts the entire CCD image vertically, in a column-parallel way, to an identical CCD completely covered with a light shield. FT CCDs have large smears because the entire image takes a millisecond to be transferred. The second approach is interline transfer (ILT). Here each pixel contains an imaging diode and a light-shield-covered storage and transfer area. Thus, an ILT CCD has a fill factor of roughly 20% or less (but can be improved over two times with microlenses) and still has some residual smear due to light leaking under the light shield. Finally, there is frame interline transfer (FIT), a combination of both FT and ILT approaches, representing a sort of one-two punch to reduce smear. The additional size of FT and FIT CCDs, due to the separate CCD array storage areas, increases die size and thus sensor cost.[3]

The unique CCD fabrication process precludes cost-efficient integration of on-chip ancillary circuits such as timing generators, clock drivers, signal processors, and analog-to-digital converters (ADCs), so that implementation of a CCD-based camera system requires an actual set of chips. This increases system power and retards miniaturization of cameras. The shift-style readout of the CCD (fundamental to its operation) does not allow the efficient readout of "windows of interest" or lower resolution readout without risking charge overflow.

Despite these functional limitations, CCDs have achieved an extraordinarily high level of performance with low readout noise, high dynamic range, and excellent responsivity. Functionality and the highly complex details of the CCD stand testament to 30 years of superb engineering evolution. Any new imaging technology, such as CMOS, must achieve similar levels of performance to displace CCD technology, or have other overwhelming advantages such as very low power or new functions.

CMOS pixels

Rather than the shift-style (raster-scan) readout of the CCD, CMOS image sensors read out the signal collected by each pixel by directly addressing it (as in a DRAM). Selecting a particular pixel (or row of pixels) for readout requires a unique set of switches to be activated. There are two approaches to pixels–passive and active.

In a passive pixel, charge collected by the pixel flows out into a column readout wire when an in-pixel switch (transistor) is selected. An amplifier at the end of the wire (at the bottom of the column) converts the sensed charge into a voltage level. Since the large-capacitance column wire collects a small amount of charge, noise becomes a critical factor. In fact, the major problems with the passive pixel are its readout noise level and scalability. Readout noise with a passive pixel falls typically in the range of 250 electrons rms, which can be compared to commercial CCDs that achieve less than 20 electrons rms of read noise. The passive pixel also does not scale well to larger array sizes and/or faster pixel readout rates. This is because both increased bus capacitance and faster readout

speeds result in higher readout noise.

The single-transistor, photodiode passive pixel allows the highest design fill factor for a given pixel size or the smallest pixel size for a given design fill factor for a particular CMOS process. A second selection transistor has sometimes been added to permit true random access addressing. The QE of the passive pixel can be quite high due to the large fill factor and absence of an overlying layer of polysilicon such as that found in many CCDs. Passive pixel sensors (PPS) have been offered by Reticon since the late 1960s with very limited on-chip electronics. Hitachi and Matsushita further investigated their use in the 1980s for camcorders. Starting in the early 1990s, CMOS PPS devices have been offered with substantial integrated electronics by VLSI Vision, and in the late 1990s by Omnivision.

In an active pixel, the amplifier is located within the pixel and typically provides charge gain between the photodetector and an analog signal processor at the bottom of each column, as illustrated in Figure 3. This way, the noise susceptibility of the passive pixel is overcome. The in-pixel amplifier enables the CMOS active pixel sensor (APS) to trade pixel fill factor for improved performance compared to passive pixels. The pixel pitch is typically between 10 and 20 times minimum feature size L, as shown in Figure 4. The amplifier is typically implemented as a single source follower because of simplicity and excellent gain uniformity. Sampled twice (known as correlated double sampling, or CDS), the pixel signal removes fixed-pattern noise and correlated temporal noise, a significant improvement introduced by the NASA Jet Propulsion Laboratory in 1993[4] to CMOS image sensors.

In CDS, taking the difference of the two samples removes the dc (offset) component from the readout signal and suppresses 1/f noise from the transistors, if the samples are closely spaced in time. (A spatially varying dc offset leads to a fixed pattern in the image, referred to as fixed-pattern noise, or FPN. Depending on its source, FPN can lead to unacceptable image artifacts such as stripes.) If the first sample is taken after the readout node resets, and the second after the signal is transferred to the readout node, CDS also suppresses reset or kTC noise. The idea of using CDS to remove noise was first applied to radar signal processing and then to CCDs beginning in the mid-1970s.

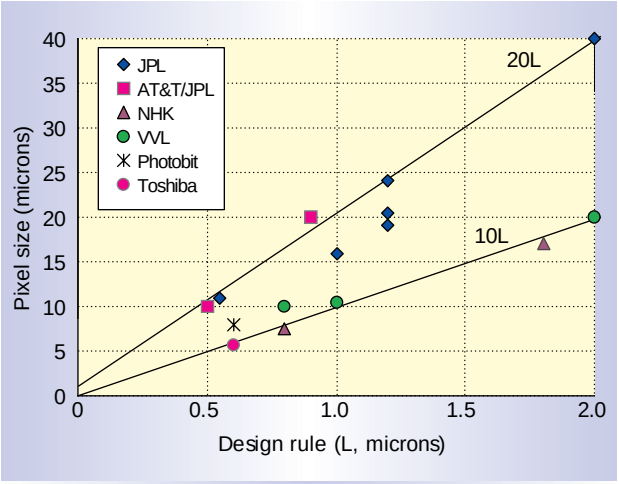

Figure 4. Scaling trend of active pixel sensors. Pixel sizes typically fall between 10 and 20 times minimum feature size L. To be cost-competitive with CCDs, most commercial applications require pixel sizes below 10 µm.

The active pixel photodetector element can be implemented in several ways, including a simple *pn* junction photodiode, a photogate structure that acts like a microCCD, a logarithmic photodetector, or a pinned photodiode. Each has various advantages and disadvantages with respect to sensitivity, noise, pixel size, and linearity, and the choice often depends on the application. Generally, active pixels have many advantages over passive pixels including lower readout noise, faster readout rates, and the ability to work well in the case of large-format (such as megapixel) arrays. We have recorded noise as low as 5 electrons rms,[5] readout speeds of 8,000 frames per second,[6] and arrays as large as 2,000 elements × 2,000 elements.

Active pixel sensors have been developed and championed by JPL for high-performance (low-noise) space applications since 1992, and have since transferred to US companies like Kodak, Motorola, Lucent, National Semiconductor, Intel, and Hewlett-Packard. Photobit, formed in 1995 by former JPL engineers, offers CMOS APS image sensors. VLSI Vision, Omnivision, and an imaging kit from Intel offer CMOS APS chips. Recently, Toshiba introduced a camera incorporating a CMOS APS. Supposedly, additional development work on CMOS APSs is underway at Rockwell, IBM, Polaroid, Hyundai, Olym-

Figure 5. JPL megapixel slow-scan CMOS APS with 1,024 analog-to-digital converters integrated on chip in a 10-µm pitch.

pus, Canon, Philips, SGS Thompson, and others, as well as in at least a dozen university laboratories.

System on a chip

The CMOS active pixel sensor achieves its greatest advantage when integrated with a variety of other support circuits.[7] In a simple sensor, only a minimal number of on-chip support circuits exist. Row and column decoders (or shift registers) select rows and pixels within the row for readout. An analog signal chain is often integrated on a simple chip to provide noise reduction and removal of artifacts such as fixed-pattern noise.

One of the key steps in realizing a digital camera on a chip is developing an on-chip ADC suitable for integration with the image sensor. There are many considerations for on-chip ADC. The ADC must support video rate data that ranges from 0.92 Msamples/s for a 320 × 288-pixel format sensor operating at 10 frames per second for videoconferencing, to 55.3 Msamples/s for a 1,280 × 720-pixel format sensor operating at 60 frames per second.

The ADC must have at least 8-bit resolution with low integral nonlinearity (INL) and differential nonlinearity (DNL) so as not to introduce distortion or artifacts into the image. The ADC can dissipate only minimal power, typically under 100 mW, to avoid introduction of hot spots with extra dark current generation. The ADC cannot consume too much chip area or it will void the economic advantage of on-chip integration. Also, the ADC cannot introduce noise into the analog imaging portion of the sensor through substrate coupling or other crosstalk mechanisms that would deteriorate image quality. Fortunately, conventional forces have driven ADC development consistent with these needs, and today, integration of a single ADC on the image sensor is feasible for many applications.

For high throughput with ultra low power dissipation, a column-parallel ADC architecture (one ADC per column, or one ADC for a group of neighboring columns) has been developed by JPL and Photobit for both the analog signal processor (ASP) and the ADC. This architecture has the advantage of high throughput and readout versatility, but requires the layout of very tall, thin circuits that must be well matched from column to column to avoid FPN. Figure 5 shows an example of a JPL sensor with 10-µm pixel pitch and 1,024 on-chip ADCs, each with 10-µm pitch.

In a full digital camera on a chip, additional digital circuitry must be incorporated to perform interface functions, provide timing and control to the sensor array and ADC, control readout, and also perform other smart functions. Figure 6 shows a digital camera on a chip with a 512 × 384-pixel array and a 7.9-µm pixel pitch.

Figure 7 shows a block diagram of the sensor. The chip is commanded over a serial interface to set up internal control registers. A 14.3-MHz master clock allows data to be read out at up to 14.3 Mbytes/s, corresponding to a 39-full-frame/s imaging rate. A central controller performs all sequencing of pixel readout, signal processing, A/D conversion, and ADC array readout. Windows of interest can be read out to allow electronic pan and tilt. A separate auto exposure block continually

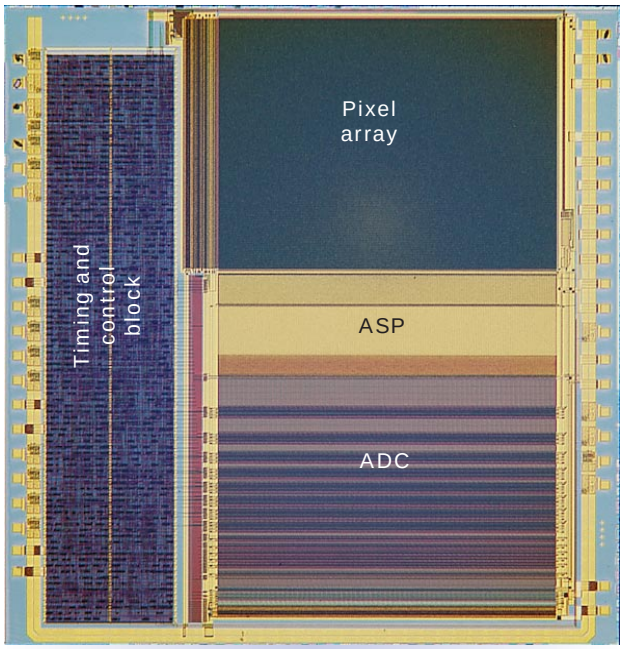

Figure 6. Photobit 1/4-inch format, 512 × 384-pixel digital color camera on a chip with pixel array, ASP, ADC, and on-chip interface, timing, control, and smart function digital block.

adjusts both the electronic shutter setting and the ADC gain setting to match the sensor's 8-bit dynamic range (limited by the ADC) to the scene. Total power dissipation of the chip is under 50 mW.

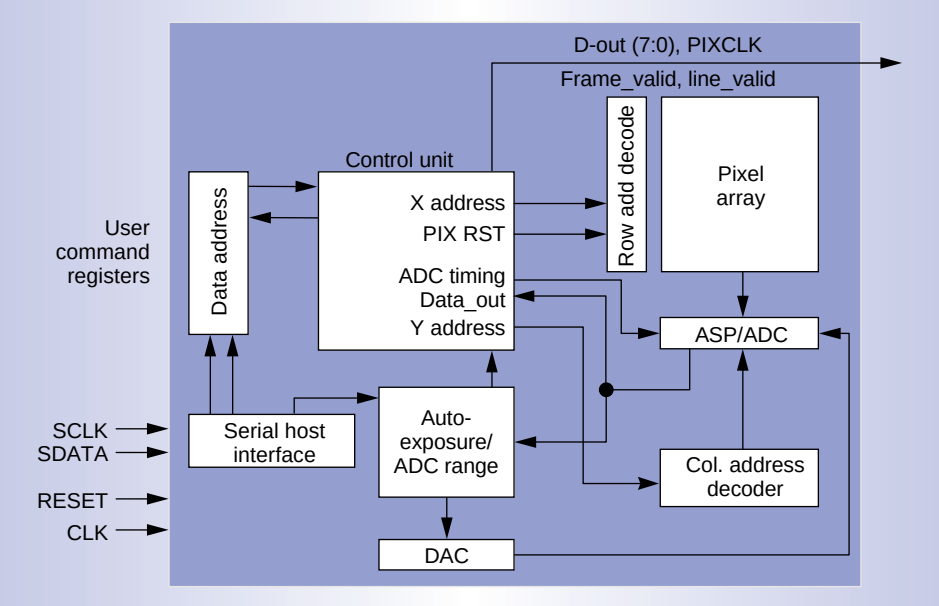

Figure 7. Block diagram of the system on a chip.

Rapid rate of progress

The development of CMOS APS image sensor technology and in particular, systems on a chip, is occurring at a rapid rate. Just a year or two ago, the commercial state of the art was represented by low-performance, monochrome, passive-pixel CMOS image sensors. In a sense, this early introduction of CMOS image sensors has hurt the technology's reputation. Such image sensor chips were useful only for toys and machine vision, where imaging performance was secondary to on-chip functionality and low power. However, more recent offerings of commercial monochrome cameras for video have seen a dramatic rise in performance. Fixed-pattern noise (such as vertical stripes of different gray levels) has nearly vanished, and temporal noise levels have dropped.

In the past year, color CMOS image sensors have emerged on the marketplace. These devices use the same on-chip CFA technology developed for CCDs. Color sensors for digital still cameras have also been developed (like the VLSI Vision 800 × 1,000-pixel APS) that are characterized by slower readout rates but higher pixel resolution and increased dynamic range.

Just emerging from several R&D efforts are true digital cameras on a chip. These sensors feature a full digital interface with no analog signals at all and will greatly simplify camera design. At the present time there are two camps in digital cameras on a chip, depending on the technology's application.

In one camp (advocates include Intel, Kodak, and Photobit), color interpolation and image compression take place off the chip in a host computer or companion video-processing chips. This approach permits adaptive processing to meet a wide variety of applications, but requires a companion chip or computer. It is a particularly important approach when the interface bandwidth is limited (for example, by USB or Firewire interface standards), since video chips produce a large amount of data, and color interpolation triples data volume. Recently, researchers at JPL described a low-power, 256 × 256-pixel sensor designed for NASA space applications. The sensor contains a serial interface for both command and data output, on-chip DACs for programmable internal biases (such as ADC reference), and self-calibrating ADCs.[8] Additionally, Photobit recently announced its 1/4-inch optical format 512 × 384-pixel digital color camera on a chip,[9] shown in Figure 6. An example image grabbed from the digital video output is shown in Figure 8.

Figure 8. Color image grabbed from 30-fps video from the chip shown in Figure 6 and processed conventionally. Cropped image resolution is approximately 350 × 370 pixels (out of 512 × 384 pixels). Source image was a laser-printer output transparency of the scanned image.

The second camp advocates putting as much of the color interpolation and other digital signal processing on the same chip as the image sensor. This is important for a variety of stand-alone applications and for direct replacement of CCD-based digital camera sys-

Figure 9. Photobit's 10 cm^2 dental X-ray sensor is in volume production for a custom-design customer. (Radiograph courtesy of Schick Technologies.)

tems. For example, workers at Matsushita described a research project in which a low-resolution sensor was integrated with ADC and DCT compression circuitry.[10] An experimental 352 × 288-pixel CMOS APS with on-chip digital color interpolation operating at 30 frames/s, and a 306 × 244-pixel single-chip color camera with analog composite color video NTSC output were described recently.[11, 12]

While much of the commercial focus has naturally been on markets such as multimedia image capture that are expected to lead to commodity-type CMOS image sensors over the next five years, many other application areas are also being explored. These include automotive applications, security and law enforcement, toys, and machine vision. For example, a VLSI Vision monochrome passive-pixel sensor was incorporated into a Tyco children's camcorder toy.

One interesting application area is in medical X rays. At the 1998 IEEE International Solid-State Circuits Conference, Photobit presented a paper on a CMOS dental X-ray chip it developed with a strategic partner over the past few years. This camera on a chip is probably one of the world's largest commercial CMOS chips, measuring over 37 mm × 28 mm (over 10 cm^2). The chip, placed in the patient's mouth, detects the onset of X-ray irradiation, integrates the X-ray image, and self-initiates the readout of the pixel data and a subsequent dark reference frame. An image appears in Figure 9.

The history of microelectronics teaches us that integration leads to greater reliability, lower system power, and plummeting system cost/performance ratios. CMOS-based imaging systems on a chip can be expected to reflect these long-standing trends as they develop over the next five years.[13] Functions such as full-color signal processing, auto white balance, auto focus, and image/video compression will be integrated onto a single chip. We can expect the emergence of a plethora of imaging applications and the insertion of image capture systems in many aspects of our personal lives. Widespread video teleconferencing is as inevitable as debates over privacy versus security.

The great battle between CCDs and CMOS APSs is just beginning as CMOS APSs begin to not only open new markets but also absorb market segments previously controlled by CCDs. CCD manufacturers can be expected to counter with cost reductions (as has already begun) and with lower power requirements. While CCD cameras could, in principle, be shrunk to two-chip solutions (CCD plus a do-all CMOS chip), improved functional capabilities and low-power advantages are fundamental to CMOS-based imaging technology. The next five years will be interesting times indeed. MICRO

References

1. R. P. Khosla, "From Photons to Bits," *Physics Today*, Vol. 45, No. 12, Dec. 1992, pp. 42-49.
2. Y. Ishihara and K. Tanigaki, "A High Sensitivity IL-CCD Image Sensor with Monolithic Resin Lens Array," *1983 IEEE Int'l Electron Devices Conf., Digest of Tech. Papers,* IEEE, Piscataway, N.J., pp. 497-500.
3. A. Theusissen, *Solid-State Imaging with Charge-Coupled Devices*, Kluwer Academic Publishers, Boston, Mass., 1995.
4. S. Mendis, S. Kemeny, and E.R. Fossum, "A 128 × 128 CMOS Active Pixel Image Sensor for Highly Integrated Imaging Systems," *1993 IEEE Int'l Electron Devices Conf.,*

Digest of Tech. Papers, IEEE, Piscataway, N.J., pp. 583-586.

5. O. Yadid-Pecht et al., "Optimization of Active Pixel Sensor Noise and Responsivity for Scientific Applications," *Proc. SPIE, Solid-State Sensor Arrays: Development and Applications*, Vol. 3019, Bellingham, Wash., 1997, pp. 125-136.
6. R. Panicacci et al., "128 Mbit/second Multiport CMOS Binary Active Pixel Image Sensor," *Proc. IEEE Int'l Solid-State Circuits Conf.*, IEEE Computer Soc. Press, Los Alamitos, Calif., Feb. 1996, pp. 100-101.
7. E.R. Fossum, "CMOS Image Sensors—Electronic Camera on a Chip," *IEEE Trans. Electron Devices*, Vol. 44, No. 10, Oct. 1997, pp. 1689-1698.
8. T. Shaw et al., "A Single-Chip CMOS APS Digital Camera," *Prog. 1997 IEEE Work. Charge-Coupled Devices and Advanced Image Sensors*, Bruges, Belgium, Jun. 5-7, 1997, pp. R24.1-R24.4.
9. R.Panicacci et al., "1/4-inch CMOS Active Pixel Sensor with Smart On-Chip Functions and Full Digital Interface," *Proc. Hot Chips IX Symp.*, contact Eric Fossum at fossum@photobit.com for a copy.
10. S. Kawahito et al., "A Compressed Digital Output CMOS Image Sensor with Analog 2-D DCT Processors and ADC Quantizer," *IEEE Int'l Solid-State Circuits Conf. Digest of Tech. Papers*, Feb. 1997, pp.184-185.
11. M. Loinaz et al., "A 200-mW 3.3-V CMOS Color Camera IC Producing 352 × 288 24-bit Video at 30 Frames/s," *IEEE Int'l Solid-State Circuits Conf. Digest of Tech. Papers*, Feb. 1998, pp. 168-169.
12. S. Smith et al., "A Single Chip 306- × 244-Pixel CMOS NTSC Video Camera," *IEEE Int'l Solid-State Circuits Conf. Digest of Tech. Papers*, IEEE CS Press, Feb. 1998, pp. 170-171.
13. P. Wong, "Technology and Scaling Considerations for CMOS Imagers," *IEEE Trans. Electron Devices*, Vol. 43, No. 12, 1996, pp. 2131-2142.

Eric R. Fossum serves as chief scientist and chairman of the board at Photobit Corporation. He has extensive experience with CCDs, APSs, and infrared focal-plane arrays, including semiconductor device microfabrication, device physics, and low-power CCD and CMOS imaging circuits. Fossum also teaches classes in image sensors at UCLA.

He has received prestigious awards, including the Yale Becton Prize, the IBM Faculty Development Award, the National Science Foundation Presidential Young Investigator Award, the JPL Lew Allen Award for Excellence, and the NASA Exceptional Achievement Medal.

Fossum received his BS in physics and engineering from Trinity College in Connecticut and his PhD in electrical engineering from Yale. He is a fellow of the IEEE and holds 10 US patents.

Direct questions concerning this article to Eric R. Fossum, Photobit Corp., 135 N. Los Robles Avenue, 7th Floor, Pasadena, CA 91101; fossum@photobit.com.