Chapter 5

Large and Fast: Exploiting Memory Hierarchy
Principle of Locality

- Programs access a small proportion of their address space at any time

- Temporal locality
  - Items accessed recently are likely to be accessed again soon
  - E.g., instructions in a loop, induction variables

- Spatial locality
  - Items near those accessed recently are likely to be accessed soon
  - E.g., sequential instruction access, array data
Taking Advantage of Locality

- Memory hierarchy
- Store everything on disk
- Copy recently accessed (and nearby) items from disk to smaller DRAM memory
  - Main memory
- Copy more recently accessed (and nearby) items from DRAM to smaller SRAM memory
  - Cache memory attached to CPU
Memory Hierarchy Levels

- Block (aka line): unit of copying
  - May be multiple words
- If accessed data is present in upper level
  - Hit: access satisfied by upper level
    - Hit ratio: hits/accesses
- If accessed data is absent
  - Miss: block copied from lower level
    - Time taken: miss penalty
    - Miss ratio: misses/accesses
      - Miss ratio: misses/accesses = 1 – hit ratio
  - Then accessed data supplied from upper level
Memory Technology

- Static RAM (SRAM)
  - 0.5ns – 2.5ns, $2000 – $5000 per GB
- Dynamic RAM (DRAM)
  - 50ns – 70ns, $20 – $75 per GB
- Magnetic disk
  - 5ms – 20ms, $0.20 – $2 per GB
- Ideal memory
  - Access time of SRAM
  - Capacity and cost/GB of disk
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Cache Memory

- Cache memory
  - The level of the memory hierarchy closest to the CPU

Given accesses $X_1, \ldots, X_{n-1}, X_n$

- How do we know if the data is present?
- Where do we look?

<table>
<thead>
<tr>
<th>$X_4$</th>
<th>$X_4$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$X_1$</td>
<td>$X_1$</td>
</tr>
<tr>
<td>$X_{n-2}$</td>
<td>$X_{n-2}$</td>
</tr>
<tr>
<td>$X_{n-1}$</td>
<td>$X_{n-1}$</td>
</tr>
<tr>
<td>$X_2$</td>
<td>$X_2$</td>
</tr>
<tr>
<td>$X_3$</td>
<td>$X_3$</td>
</tr>
</tbody>
</table>

a. Before the reference to $X_n$  b. After the reference to $X_n$
Direct Mapped Cache

- Location determined by address
- Direct mapped: only one choice
  - (Block address) modulo (#Blocks in cache)

- #Blocks is a power of 2
- Use low-order address bits
Hash Function: LS Block Address bits

- Tag bits for each block must be stored in the cache in order to identify which of the multiple blocks that hash in the same slot is currently in that slot.
- Neighbour blocks do not collide.
- Neighbour blocks will usually collide.
Tags and Valid Bits

- How do we know which particular block is stored in a cache location?
  - Store block address as well as the data
  - Actually, only need the high-order bits
  - Called the tag

- What if there is no data in a location?
  - Valid bit: 1 = present, 0 = not present
  - Initially 0
Cache Example

- 8-blocks, 1 word/block, direct mapped
- Initial state

<table>
<thead>
<tr>
<th>Index</th>
<th>V</th>
<th>Tag</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>N</td>
<td></td>
<td></td>
</tr>
<tr>
<td>001</td>
<td>N</td>
<td></td>
<td></td>
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<td>010</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>011</td>
<td>N</td>
<td></td>
<td></td>
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<tr>
<td>100</td>
<td>N</td>
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<tr>
<td>101</td>
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<td></td>
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<tr>
<td>110</td>
<td>N</td>
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## Cache Example

<table>
<thead>
<tr>
<th>Word addr</th>
<th>Binary addr</th>
<th>Hit/miss</th>
<th>Cache block</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>10 110</td>
<td>Miss</td>
<td>110</td>
</tr>
</tbody>
</table>

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</tr>
<tr>
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<td></td>
<td></td>
</tr>
<tr>
<td><strong>110</strong></td>
<td>Y</td>
<td><strong>10</strong></td>
<td>Mem[10110]</td>
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<tr>
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<tbody>
<tr>
<td>26</td>
<td>11 010</td>
<td>Miss</td>
<td>010</td>
</tr>
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<tr>
<td>16</td>
<td>10 000</td>
<td>Miss</td>
<td>000</td>
</tr>
<tr>
<td>3</td>
<td>00 011</td>
<td>Miss</td>
<td>011</td>
</tr>
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</tr>
<tr>
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<td>Y</td>
<td>00</td>
<td>Mem[00011]</td>
</tr>
<tr>
<td>100</td>
<td>N</td>
<td></td>
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</table>
Address Subdivision

Address (showing bit positions)

63 62  ···  13 12  11  ···  2  1  0

Byte offset

Index

Valid

Tag

Data

Index

0

1

2

...

Data

52

10

32

52

Hit

Tag

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Average Access Time

- Hit time is also important for performance
- Average memory access time (AMAT)
  - $AMAT = \text{Hit time} + \text{Miss rate} \times \text{Miss penalty}$
- Example
  - CPU with 1ns clock, hit time = 1 cycle, miss penalty = 20 cycles, L-cache miss rate = 5%
  - $AMAT = 1 + 0.05 \times 20 = 2\text{ns}$
    - 2 cycles per instruction
Measuring Cache Performance

- Components of CPU time
  - Program execution cycles
    - Includes cache hit time
  - Memory stall cycles
    - Mainly from cache misses
- With simplifying assumptions:

\[
\text{Memory stall cycles} = \frac{\text{Memory accesses}}{\text{Program}} \times \text{Miss rate} \times \text{Miss penalty}
\]

\[
= \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Misses}}{\text{Instruction}} \times \text{Miss penalty}
\]
Cache Performance Example

Given
- I-cache miss rate = 2%
- D-cache miss rate = 4%
- Miss penalty = 100 cycles
- Base CPI (ideal cache) = 2
- Load & stores are 36% of instructions

Miss cycles per instruction
- I-cache: \(0.02 \times 100 = 2\)
- D-cache: \(0.36 \times 0.04 \times 100 = 1.44\)

Actual CPI = 2 + 2 + 1.44 = 5.44

Ideal CPU is 5.44/2 = 2.72 times faster
Performance Summary

- When CPU performance increased
  - Miss penalty becomes more significant
- Decreasing base CPI
  - Greater proportion of time spent on memory stalls
- Increasing clock rate
  - Memory stalls account for more CPU cycles
- Can’t neglect cache behavior when evaluating system performance
Increased Line (Block) Size, to exploit Spatial Locality

Example:
- Line (Block) Size = 4 Words = 16 Bytes
- Cache Size = 128 Bytes = 8 Lines (Blocks)

- Lines (blocks) are always ‘properly’ Aligned
- All or none words in Line brought in Cache

Conceptual ‘Horizontal’ layout of the words in a Line

Numbers inside boxes are addresses – not contents
‘Vertical’ Layout of the Words in a Line(Block)

- Line Size = 4 Words = 16 Bytes
- Cache Size = 128 Bytes = 8 Lines

Same example:

- Address
- Tag
- Line Index
- Line & Word Index
- Byte in Word
- Data
- Tag
- Vertical Layout of the Words in a Line(Block)
Block Size Considerations

- Larger blocks should reduce miss rate
  - Due to spatial locality
- But in a fixed-sized cache
  - Larger blocks $\Rightarrow$ fewer of them
    - More competition $\Rightarrow$ increased miss rate
  - Larger blocks $\Rightarrow$ pollution
- Larger miss penalty
  - Can override benefit of reduced miss rate
  - Early restart and critical-word-first can help

They also reduce the number of Tags, hence speed up Tag look-up
FIGURE 5.11 Miss rate versus block size. Note that the miss rate actually goes up if the block size is too large relative to the cache size. Each line represents a cache of different size. (This figure is independent of associativity, discussed soon.) Unfortunately, SPEC CPU2000 traces would take too long if block size were included, so these data are based on SPEC92.
Example: Intrinsity FastMATH

- Embedded MIPS processor
  - 12-stage pipeline
  - Instruction and data access on each cycle
- Split cache: separate I-cache and D-cache
  - Each 16KB: 256 blocks × 16 words/block
  - D-cache: write-through or write-back
- SPEC2000 miss rates
  - I-cache: 0.4%
  - D-cache: 11.4%
  - Weighted average: 3.2%
Example: Intrinsity FastMATH

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Cache Misses

- On cache hit, CPU proceeds normally
- On cache miss
  - Stall the CPU pipeline (on I-cache miss, can also let the rest of the pipeline proceed to completion)
  - Fetch block from next level of hierarchy
  - Instruction cache miss
    - Restart instruction fetch
  - Data cache miss
    - Complete data access

Out-of-Order Pipelines do not stall the pipeline, but look for subsequent instructions that do not depend on the miss data; their D-cache must support one or more outstanding misses
Write-Through

- On data-write hit, could just update the block in cache
  - But then cache and memory would be inconsistent
- Write through: also update memory
- But makes writes take longer
  - e.g., if base CPI = 1, 10% of instructions are stores, write to memory takes 100 cycles
    - Effective CPI = 1 + 0.1 \times 100 = 11
- Solution: write buffer
  - Holds data waiting to be written to memory
  - CPU continues immediately
    - Only stalls on write if write buffer is already full

Write-Combining: sequential accesses to DRAM take shorter for subsequent words beyond the first one
Write-Back  Ετερόχρονη Εγγραφή

- Alternative: On data-write hit, just update the block in cache
  - Keep track of whether each block is dirty

- When a dirty block is replaced
  - Write it back to memory
  - Can use a write buffer to allow replacing block to be read first

Main Memory is inconsistent with Cache

We will revisit this when talking about I/O, then about multicores…
Write Allocation

- What should happen on a write miss?
  - Alternatives for write-through
    - Allocate on miss: fetch the block
    - Write around: don’t fetch the block
      - Since programs often write a whole block before reading it (e.g., initialization)
  - For write-back
    - Usually fetch the block

Several modern processors allow software to control this policy on a per-page granularity (via page-table flag)
Associative Caches

- Fully associative
  - Allow a given block to go in any cache entry
  - Requires all entries to be searched at once
  - Comparator per entry (expensive)

- n-way set associative
  - Each set contains $n$ entries
  - Block number determines which set
    - (Block number) modulo (#Sets in cache)
  - Search all entries in a given set at once
  - $n$ comparators (less expensive)
**Associative Cache Example**

- **Direct mapped**
  - Block #: 0, 1, 2, 3, 4, 5, 6, 7
  - Data
  - Tag: 1, 2
  - Search

- **Set associative**
  - Set #: 0, 1, 2, 3
  - Data
  - Tag: 1, 2
  - Search

- **Fully associative**
  - Data
  - Tag: 1, 2
  - Search

---

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Spectrum of Associativity

- For a cache with 8 entries

One-way set associative
(direct mapped)

Block | Tag | Data
--- | --- | ---
0 | | |
1 | | |
2 | | |
3 | | |
4 | | |
5 | | |
6 | | |
7 | | |

Two-way set associative

Set | Tag | Data | Tag | Data
--- | --- | --- | --- | ---
0 | | | |
1 | | | |
2 | | | |
3 | | | |

Four-way set associative

Set | Tag | Data | Tag | Data | Tag | Data | Tag | Data
--- | --- | --- | --- | --- | --- | --- | --- | ---
0 | | | | | | | | |
1 | | | | | | | | |

Eight-way set associative (fully associative)

Tag | Data | Tag | Data | Tag | Data | Tag | Data | Tag | Data | Tag | Data | Tag | Data | Tag | Data
--- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | ---
## Associativity Example

- Compare 4-block caches
  - Direct mapped, 2-way set associative, fully associative
  - Block access sequence: 0, 8, 0, 6, 8
- Direct mapped

### Table: Cache Access Results

<table>
<thead>
<tr>
<th>Block address</th>
<th>Cache index</th>
<th>Hit/miss</th>
<th>Cache content after access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>miss</td>
<td>Mem[0]</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>miss</td>
<td>Mem[8]</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>miss</td>
<td>Mem[0]</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>miss</td>
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<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
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</table>
### Associativity Example

#### 2-way set associative

Block access seq.: 0, 8, 0, 6, 8

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</tr>
<tr>
<td>6</td>
<td>0</td>
<td>miss</td>
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</tbody>
</table>

#### Fully associative

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</tr>
<tr>
<td>0</td>
<td>hit</td>
<td>Mem[0] Mem[8]</td>
</tr>
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</table>
How Much Associativity

- Increased associativity decreases miss rate
  - But with diminishing returns
- Simulation of a system with 64KB D-cache, 16-word blocks, SPEC2000
  - 1-way: 10.3%
  - 2-way: 8.6%
  - 4-way: 8.3%
  - 8-way: 8.1%
Set Associative Cache Organization

Address
31 30 ⋯ 12 11 10 9 8 ⋯ 3 2 1 0

Tag
Index

Index
0
1
2

253
254
255

V
Tag
Data

V
Tag
Data

V
Tag
Data

V
Tag
Data

4-to-1 multiplexer

Hit
Data
Replacement Policy

- Direct mapped: no choice
- Set associative
  - Prefer non-valid entry, if there is one
  - Otherwise, choose among entries in the set
- Least-recently used (LRU)
  - Choose the one unused for the longest time
    - Simple for 2-way, manageable for 4-way, too hard beyond that
- Random
  - Gives approximately the same performance as LRU for high associativity
Multilevel Caches

- Primary cache attached to CPU
  - Small, but fast
- Level-2 cache services misses from primary cache
  - Larger, slower, but still faster than main memory
- Main memory services L-2 cache misses
- Some high-end systems include L-3 cache
Multilevel Cache Example

Given
- CPU base CPI = 1, clock rate = 4GHz
- Miss rate/instruction = 2%
- Main memory access time = 100ns

With just primary cache
- Miss penalty = 100ns/0.25ns = 400 cycles
- Effective CPI = 1 + 0.02 \times 400 = 9
Example (cont.)

- Now add L-2 cache
  - Access time = 5ns
  - Global miss rate to main memory = 0.5%

Primary miss with L-2 hit
  - Penalty = 5ns/0.25ns = 20 cycles

Primary miss with L-2 miss
  - Extra penalty = 400 cycles
  - CPI = 1 + 0.02 \times 20 + 0.005 \times 400 = 3.4
  - Performance ratio = 9/3.4 = 2.6
Multilevel Cache Considerations

- Primary cache
  - Focus on minimal hit time

- L-2 cache
  - Focus on low miss rate to avoid main memory access
  - Hit time has less overall impact

- Results
  & often fewer ways (smaller associativity)
  - L-1 cache usually smaller than a single cache
  - L-1 block size smaller than L-2 block size
Interactions with Advanced CPUs

- Out-of-order CPUs can execute instructions during cache miss
  - Pending store stays in load/store unit
  - Dependent instructions wait in reservation stations
    - Independent instructions continue
- Effect of miss depends on program data flow
  - Much harder to analyse
  - Use system simulation
Interactions with Software

- Misses depend on memory access patterns
  - Algorithm behavior
  - Compiler optimization for memory access