Pipelined Datapath & Control Operation
without data or control dependencies, yet

University of Crete
Dept. of Computer Science
CS–225 (HY–225)
Computer ORganization
Spring 2020 semester

Slides for §9.3 – 9.5

§9.3 Pipelined Datapath Operation
§9.4 Control for the Pipelined Datapath
§9.5 Graphical representation: time–work
60: `ld x10, 40(x1)`
64: `sub x11, x2, x3`
68: `add x12, x3, x4`
72: `ld x13, 48(x1)`
76: `add x14, x5, x6`
60: `ld x10, 40(x1)`
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76: `add x14, x5, x6`

---

End of Cycle 1

---

<table>
<thead>
<tr>
<th>x1</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>x2</td>
<td>200</td>
</tr>
<tr>
<td>x3</td>
<td>300</td>
</tr>
<tr>
<td>x4</td>
<td>400</td>
</tr>
</tbody>
</table>
Start of Cycle 2

60: \texttt{ld x10, 40(x1)}
64: \texttt{sub x11, x2, x3}
68: \texttt{add x12, x3, x4}
72: \texttt{ld x13, 48(x1)}
76: \texttt{add x14, x5, x6}

\begin{tabular}{|c|}
\hline
x1 & 100 \\
\hline
x2 & 200 \\
\hline
x3 & 300 \\
\hline
x4 & 400 \\
\hline
\end{tabular}
60: \text{ld} \ x_{10}, \ 40(x_{1})
64: \text{sub} \ x_{11}, \ x_{2}, \ x_{3}
68: \text{add} \ x_{12}, \ x_{3}, \ x_{4}
72: \text{ld} \ x_{13}, \ 48(x_{1})
76: \text{add} \ x_{14}, \ x_{5}, \ x_{6}

\begin{array}{|c|c|c|c|}
\hline
x_{1} & 100 \\
\hline
x_{2} & 200 \\
\hline
x_{3} & 300 \\
\hline
x_{4} & 400 \\
\hline
\end{array}


Start of Cycle 3

60: `ld x10, 40(x1)`
64: `sub x11, x2, x3`
68: `add x12, x3, x4`
72: `ld x13, 48(x1)`
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60: `ld x10, 40(x1)`
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68: `add x12, x3, x4`
72: `ld x13, 48(x1)`
76: `add x14, x5, x6`

|x| 100 |
---|---|
x1 |     |
|x| 200 |
---|---|
x2 |     |
|x| 300 |
---|---|
x3 |     |
|x| 400 |
---|---|
x4 |     |

Control

```
add
sub
```

```
| op | f7 |
---|---|
| add |     |
```

```
| rs2 | rs1 |
---|---|
|     |     |
```

```
| IMM | IR |
---|---|
| A   | IR |
```

```
| RF   | ALU |
---|---|
|     |     |
```

```
| PC   | IMM |
---|---|
| 72   | 68 |
```

```
| +4   | PC |
---|---|
|     | 72 |
```

```
| br/jmp addr. |
---|---|
|     |     |
```

```
| we rd | Dout |
---|---|
| Addr  |     |
```

```
| Addr | DM |
---|---|
| we rd | Din |
```

```
| 100 |
---|---|
| B   |     |
```

```
| 140 |
---|---|
|     |     |
```

```
| 40  |
---|---|
| Imm |
```

```
| 300 |
---|---|
| x3  |     |
```

```
| 200 |
---|---|
| x2  |     |
```

```
| 100 |
---|---|
| A   |     |
```

```
| f3 |
---|---|
|     |
```

```
| f7 |
---|---|
|     |
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Start of Cycle 4
60: `ld x10, 40(x1)`
64: `sub x11, x2, x3`
68: `add x12, x3, x4`
72: `ld x13, 48(x1)`
76: `add x14, x5, x6`

<table>
<thead>
<tr>
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<th>x3</th>
<th>x4</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
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<td>200</td>
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<tr>
<td>72</td>
<td>400</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

End of Cycle 4
60: `ld x10, 40(x1)`
64: `sub x11, x2, x3`
68: `add x12, x3, x4`
72: `ld x13, 48(x1)`
76: `add x14, x5, x6`

Start of Cycle 5
60: `ld x10, 40(x1)`
64: `sub x11, x2, x3`
68: `add x12, x3, x4`
72: `ld x13, 48(x1)`
76: `add x14, x5, x6`

**End of Cycle 5**
60: $\text{ld } x10, 40(x1)$
64: $\text{sub } x11, x2, x3$
68: $\text{add } x12, x3, x4$
72: $\text{sd } x13, 48(x1)$
76: $\text{add } x14, x5, x6$

Cycle 2

Control

IR

PC

IM

RF

ALU

Addr

Dout

Din

DM

we

rd

br/jmp addr.
60: `ld x10, 40(x1)`
64: `sub x11, x2, x3`
68: `add x12, x3, x4`
72: `sd x13, 48(x1)`
76: `add x14, x5, x6`
60: \textit{ld} x10, 40(x1)
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Cycle 5

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60: `ld` `x10, 40(x1)`
64: `sub` `x11, x2, x3`
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Cycle 1

60: `ld x10, 40(x1)`
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### Cycle 3

- **Instr. Fetch**
- **Reg.Rd; Op**
- **ALU**
- **Data Mem.**
- **Write Back**

**Control Signal Flow**

- `sub`
- `op` to `f3`
- `rd` to `rs1`
- `rs2` to `f7`
- `PC` to `IR`
- `IR` to `add`
- `add` to `sub`
- `sub` to `Imm`
- `Imm` to `ALU`
- `ALU` to `Dout`
- `Dout` to `Data Mem.
- `Data Mem.` to `Write Back`
- `Write Back` to `Instr. Fetch`

**Diagram Details**

- **PC**
- **IM**
- **IR**
- **RF**
- **ALU**
- **Addr**
- **Din**
- **DM**

**Cycle 3 Diagram**

- Work
- Cycle 3
- `f7`
- `rd`
- `we`
- `Din`
- `rf`
- `Imm`
- `rd` to `rs1`
- `rs2` to `f7`
- `Imm` to `ALU`
- `ALU` to `Dout`
- `Dout` to `Data Mem.
- `Data Mem.` to `Write Back`
- `Write Back` to `Instr. Fetch`
60: `ld  x10, 40(x1)`
64: `sub x11, x2, x3`
68: `add x12, x3, x4`
72: `ld  x13, 48(x1)`
76: `add x14, x5, x6`

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**Cycle 4**

**Instr. Fetch** | **Reg.Rd; Op** | **ALU** | **Data Mem.** | **Write Back**
--- | --- | --- | --- | ---
**Instr. Fetch** | **Reg.Rd; Op** | **ALU** | **Data Mem.** | **Instr. Fetch**

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Diagram showing the pipeline stages of instruction execution with labels for `IM`, `IR`, `RF`, `ALU`, and `Data Mem.`, along with control signals and data flow through the pipeline stages.
60: \texttt{ld x10, 40(x1)}
64: \texttt{sub x11, x2, x3}
68: \texttt{add x12, x3, x4}
72: \texttt{ld x13, 48(x1)}
76: \texttt{add x14, x5, x6}

```plaintext
Cycle 5
```

```
Instr. Fetch | Reg.Rd; Op | ALU |
Instr. Fetch |
```