

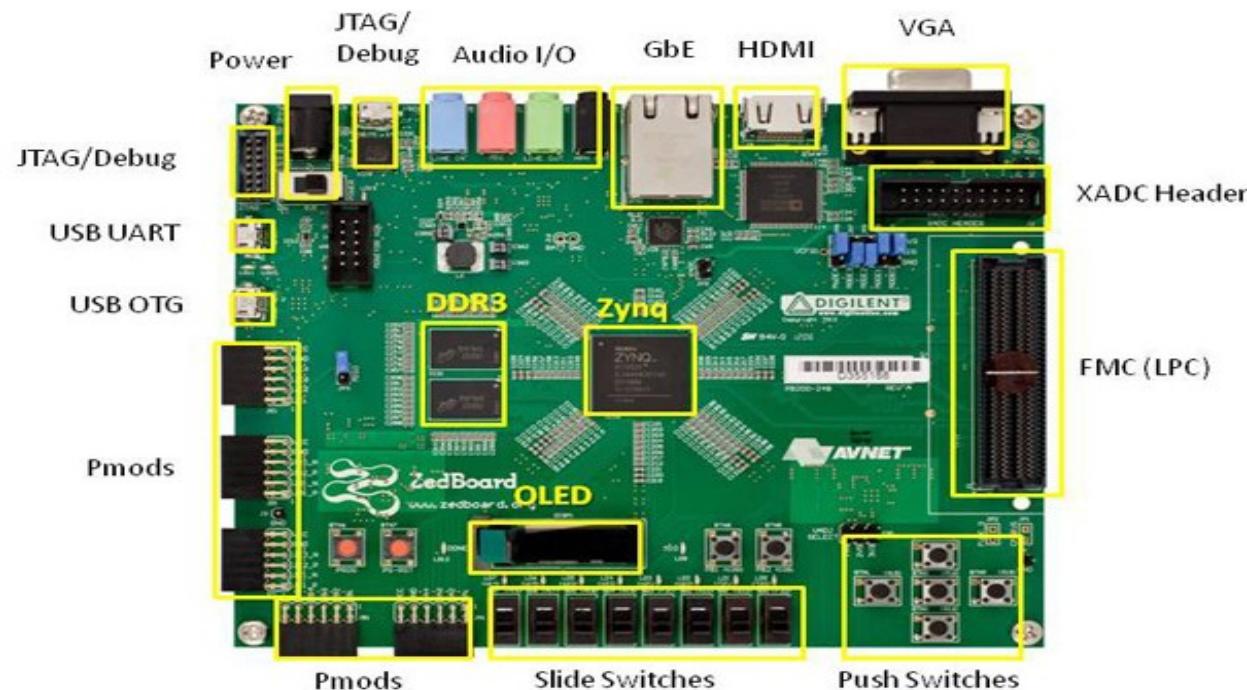
Introduction to hardware design



Sotiris Totomis
CS-220 (Spring '24)

FPGAs

- A Field Programmable Gate Array is a re-configurable circuit
- Hardware Description Languages (HDLs)



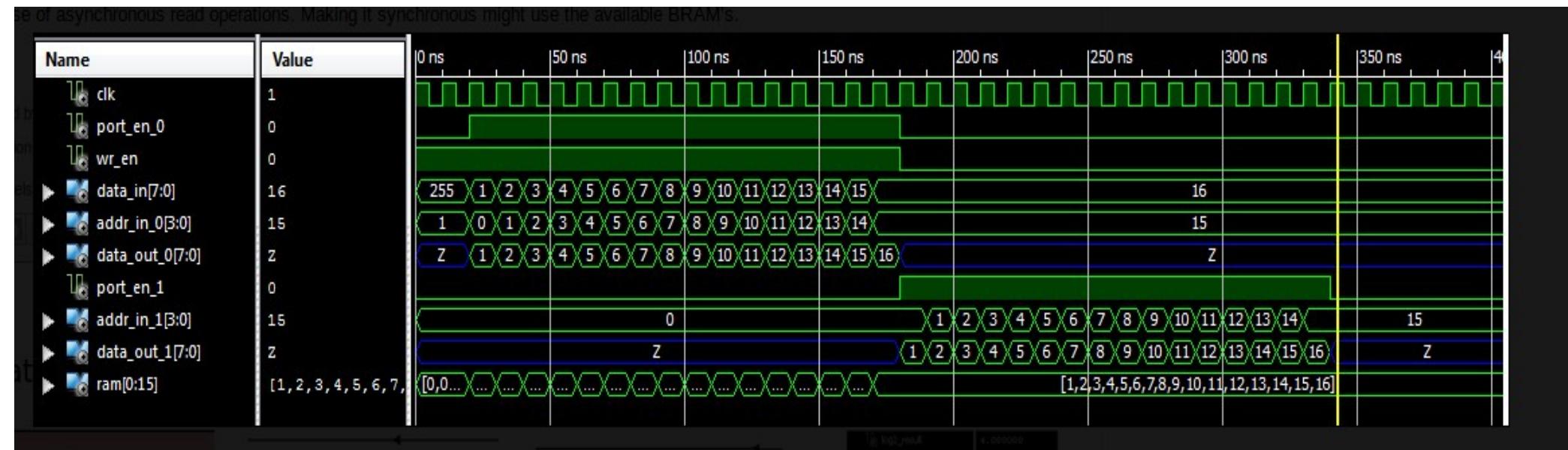
* SD card cage and QSPI Flash reside on backside of board

Vivado Design Suite

- Developed by Xilinx (now AMD)
- Vivado is suitable for
 - Simulation
 - Synthesisof HDL (SystemVerilog) designs

Simulation

- The simulation of a circuit displays circuit's behavior to hardware (HW) designers
- Why do we need a testbench (TB) for that?



Synthesis

- Transforms Register Transfer Level (RTL) designs to logic gates
- Look-Up Tables (LUTs)



Vivado Installation

- Dependencies for Linux machines
 - sudo apt install libtinfo5
 - sudo apt install libncurses5
- Linux installation
 - sudo ./xsetup
- Windows installation
 - xsetup.exe

Vivado Installation (cont'd)

Version

2023.2

2023.1

2022.2

2022.1

Vivado Archive

ISE Archive

CAE Vendor Libraries

Archive

We strongly recommend using the latest releases available.

2021

2021.1

2021.2

2020

2020.3

2020.2

2020.1

2019

2019.2

2019.1

2018

2018.3

2018.2

2018.1

Vivado Installation (cont'd)

Vivado Design Suite - HLx Editions - 2018.3 Full Product Installation

Important

We strongly recommend to use the web installers as it reduces download time and saves significant disk space.

Please see [Installer Information](#) for details.

Note: Download verification is only supported with Google Chrome and Microsoft Edge web browsers.

 [Vivado HLx 2018.3: All OS installer Single-File Download \(TAR/GZIP - 18.97 GB\)](#)

MD5 SUM Value : 8a3a75f26d0e20de21fc673ad9d40d0f

Download Verification (i)

Digests

Signature

Public Key

Download Includes

Vivado Design Suite HLx Editions (All Editions)

Download Type

Full Product Installation

Last Updated

Dec 10, 2018

Answers

[2018.x - Vivado Known Issues](#)

Documentation

[Release Notes](#)

Support Forums

[Installation and Licensing](#)

Vivado Installation (cont'd)

Vivado 2018.3 Installer - Welcome

 **Welcome**

We are glad you've chosen Xilinx as your platform development partner. This program can install the Vivado Design Environment, Software Development Kit and Documentation Navigator.

Supported operating systems for Vivado 2018.3 are:

- Windows 7.1: 64-bit
- Windows 10 Professional versions 1803 and 1809: 64-bit
- Red Hat Enterprise Linux 6.6-6.9: 64-bit
- Red Hat Enterprise Linux 7.2-7.5: 64-bit
- CentOS Linux 6.6-6.9: 64-bit
- CentOS Linux 7.2-7.5: 64-bit
- SUSE Enterprise Linux 11.4: 64-bit
- SUSE Enterprise Linux 12.3: 64-bit
- Ubuntu Linux 16.04.4 and 18.04 LTS: 64-bit - Additional library installation required

Note: This release requires upgrading your license server tools to the Flex 11.14.1 versions. Please confirm with your license admin that the correct version of the license server tools are installed and available, before running the tools.

Note: This installation program will not install cable drivers on Linux. This item will need to be installed separately, with administrative privileges.

To reduce installation time, we recommend that you disable any anti-virus software before continuing.



Copyright © 1986-2019 Xilinx, Inc. All rights reserved.

[Preferences](#) [< Back](#) [Next >](#) [Cancel](#)

Vivado Installation (cont'd)

Vivado 2018.3 Installer - Accept License Agreements

Accept License Agreements

Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.

Xilinx Inc. End User License Agreement

By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

I Agree

WebTalk Terms And Conditions

By checking "I AGREE" below, I also confirm that I have read [Section 13 of the terms and conditions](#) above concerning WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at <https://www.xilinx.com/products/design-tools/webtalk.html>. I understand that I am able to disable WebTalk later if certain criteria described in Section 13(c) apply. If they don't apply, I can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to the internet. If I fail to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of information, I agree to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 13(b).

I Agree

Third Party Software End User License Agreement

By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

I Agree

Copyright © 1986-2019 Xilinx, Inc. All rights reserved.

[< Back](#) [Next >](#) [Cancel](#)

Vivado Installation (cont'd)

Vivado 2018.3 Installer - Select Edition to Install

 XILINX®

Select Edition to Install

Select an edition to continue installation. You will be able to customize the content in the next page.

Vivado HL WebPACK
Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition. Users can optionally add Model Composer and System Generator for DSP to this installation.

Vivado HL Design Edition
Vivado HL Design Edition includes the full complement of Vivado Design Suite tools for design, including C-based design with Vivado High-Level Synthesis, implementation, verification and device programming. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add Model Composer to this installation.

Vivado HL System Edition
Vivado HL System Edition is a superset of Vivado HL Design Edition with the addition of System Generator for DSP. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add Model Composer to this installation.

Documentation Navigator (Standalone)
Xilinx Documentation Navigator (DocNav) provides access to Xilinx technical documentation both on the Web and on the Desktop. This is a standalone installation without Vivado Design Suite.

Copyright © 1986-2019 Xilinx, Inc. All rights reserved.

[< Back](#) [Next >](#) [Cancel](#)

Vivado Installation (cont'd)

Vivado 2018.3 Installer - Vivado HL WebPACK

Vivado HL WebPACK

Customize your installation by (de)selecting items in the tree below. Moving cursor over selections below provide additional information.

Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition. Users can optionally add Model Composer and System Generator for DSP to this installation.

Design Tools

- Vivado Design Suite
 - Vivado
 - System Generator for DSP
 - Model Composer
- Software Development Kit (SDK)
 - SDK Core Tools
 - Compiler Tool Chains
 - DocNav

Devices

- Production Devices
 - SoCs
 - Zynq-7000 ([limited support](#))
 - Zynq UltraScale+ MPSoC ([limited support](#))
 - Zynq UltraScale+ RFSoC
 - 7 Series ([limited support](#))
 - Artix-7
 - Kintex-7
 - Spartan-7
 - Virtex-7
 - UltraScale ([limited support](#))
 - Kintex UltraScale
 - Virtex UltraScale
 - UltraScale+ ([limited support](#))
 - Kintex UltraScale+
 - Virtex UltraScale+
 - Virtex UltraScale+ HBM
- Engineering Sample Devices

Installation Options

- NOTE: Cable Drivers are not installed on Linux. Please follow the instructions in UG973 to install Linux cable drivers
- Enable WebTalk for Vivado to send usage statistics to Xilinx (Always enabled for WebPACK license)
- Enable WebTalk for SDK to send usage statistics to Xilinx

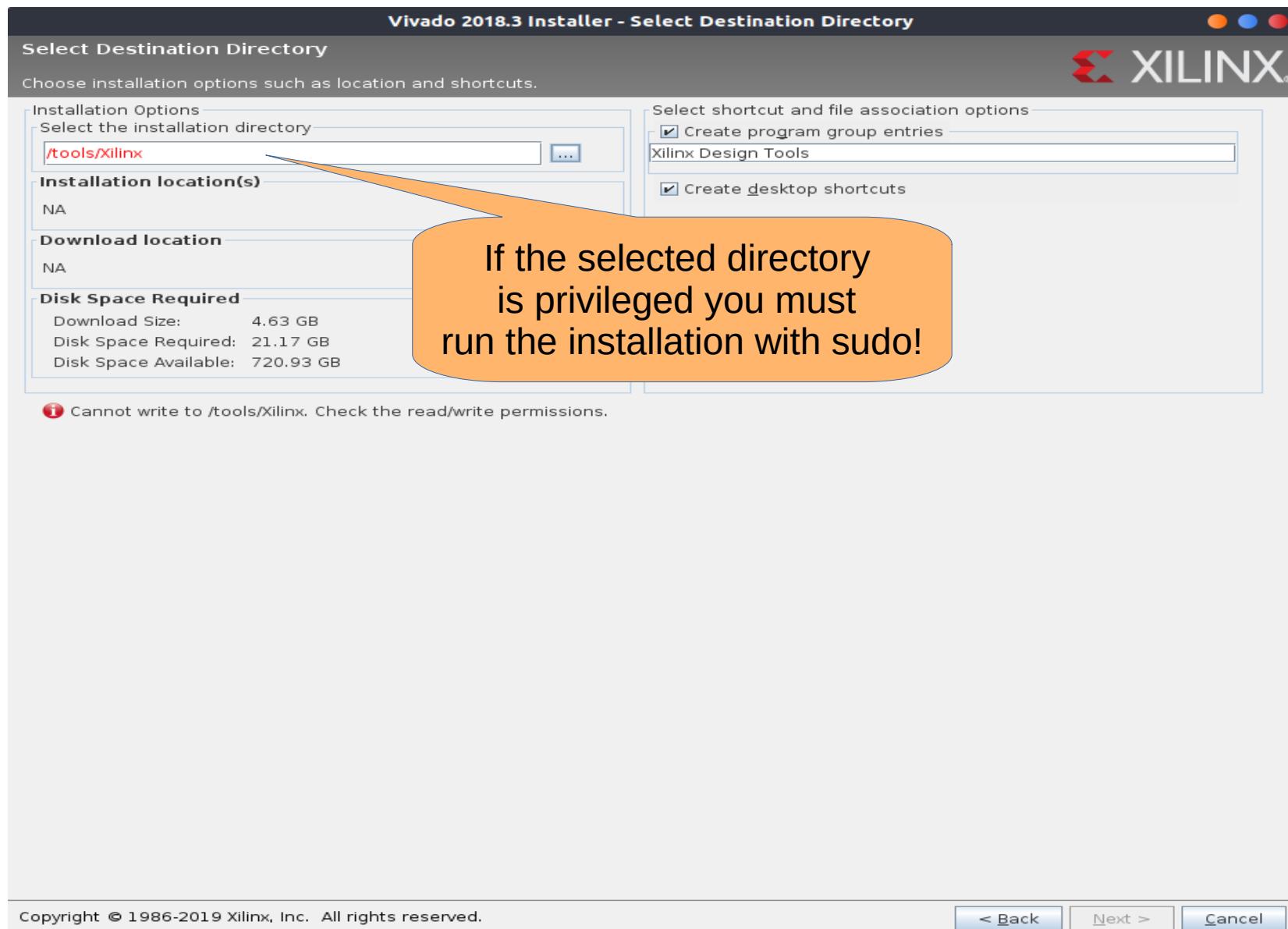
Download Size: 4.63 GB

Disk Space Required: 21.17 GB

Copyright © 1986-2019 Xilinx, Inc. All rights reserved.

12 / 30

Vivado Installation (cont'd)



If the selected directory
is privileged you must
run the installation with sudo!

! Cannot write to `/tools/Xilinx`. Check the read/write permissions.

Vivado Installation (cont'd)

Vivado 2018.3 Installer - Installation Summary

Installation Summary

Edition: Vivado HL WebPACK

Devices

- Production Devices (SoCs, 7 Series)

Design Tools

- Vivado Design Suite (Vivado)

Installation Options

- Enable WebTalk for Vivado to send usage statistics to Xilinx (Always enabled for WebPACK license)

Installation location

- /home/sototo/Vivado/2018.3

Download location

- /home/sototo/Downloads/Vivado_2018.3

Disk Space Required

- Download Size: 4.63 GB
- Disk Space Required: 21.17 GB

XILINX.

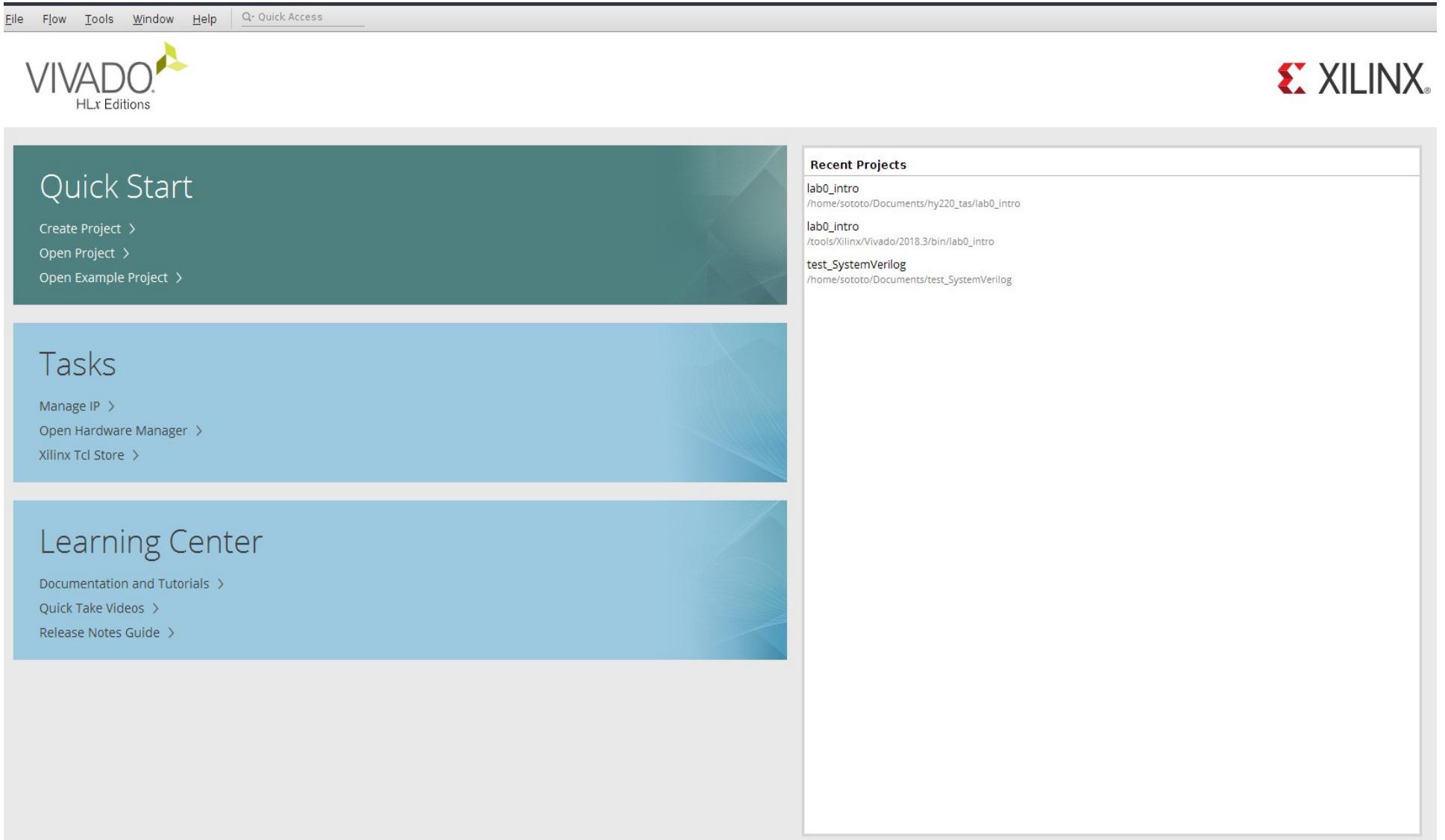
Copyright © 1986-2019 Xilinx, Inc. All rights reserved.

Preferences < Back Install Cancel

Sourcing settings to path

- Before executing Vivado through command line you have to source its settings
 - `cd installation_path/Xilinx/Vivado/2018.3`
 - `source settings64.sh`
- After this you can execute Vivado GUI by typing
 - `vivado`

Creating a project



The screenshot shows the Vivado HLx Editions software interface. The top navigation bar includes File, Flow, Tools, Window, Help, and a Quick Access search bar. The interface is divided into several sections:

- Quick Start:** Contains links for Create Project >, Open Project >, and Open Example Project >.
- Recent Projects:** Lists recent projects with their paths:
 - lab0_intro /home/sototo/Documents/hy220_tas/lab0_intro
 - lab0_intro /tools/Xilinx/Vivado/2018.3/bin/lab0_intro
 - test_SystemVerilog /home/sototo/Documents/test_SystemVerilog
- Tasks:** Contains links for Manage IP >, Open Hardware Manager >, and Xilinx Tcl Store >.
- Learning Center:** Contains links for Documentation and Tutorials >, Quick Take Videos >, and Release Notes Guide >.

Creating a project (cont'd)

New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name: ...

Project location: ...

Create project subdirectory

Project will be created at: /tools/Xilinx/Vivado/2018.3/bin/test

? < Back Next > Finish Cancel

Creating a project (cont'd)

New Project

Project Type
Specify the type of project to create.



- RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
 Do not specify sources at this time
- Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
 Do not specify sources at this time
- I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
- Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
- Example Project
Create a new Vivado project from a predefined template.

[?](#) [< Back](#) [Next >](#) [Finish](#) [Cancel](#)

Creating a project (cont'd)

New Project

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.



Use Add Files, Add Directories or Create File buttons below

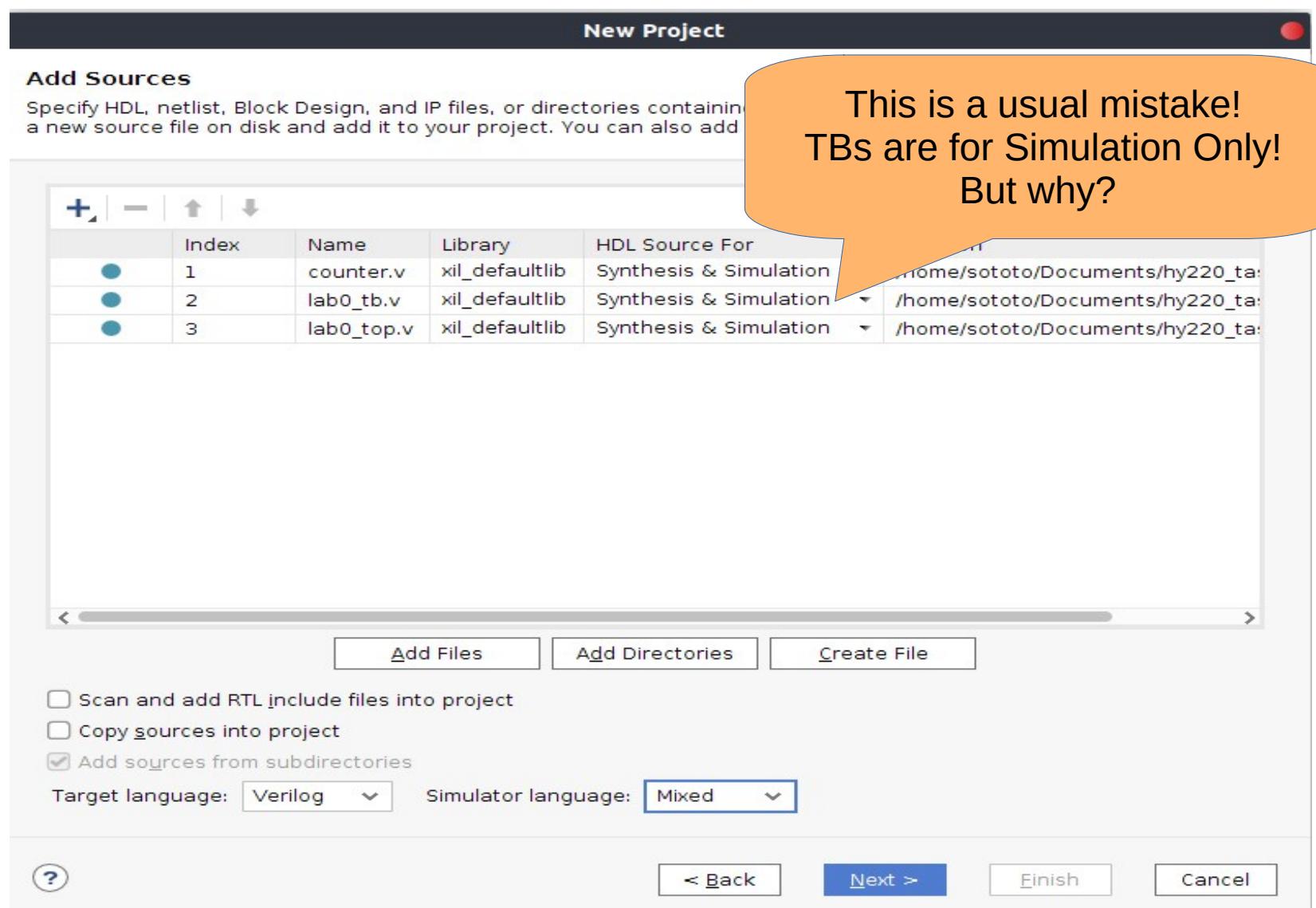
Add Files **Add Directories** **Create File**

Scan and add RTL include files into project
 Copy sources into project
 Add sources from subdirectories

Target language: **Verilog** Simulator language: **Mixed**

? **< Back** **Next >** **Finish** **Cancel**

Creating a project (cont'd)



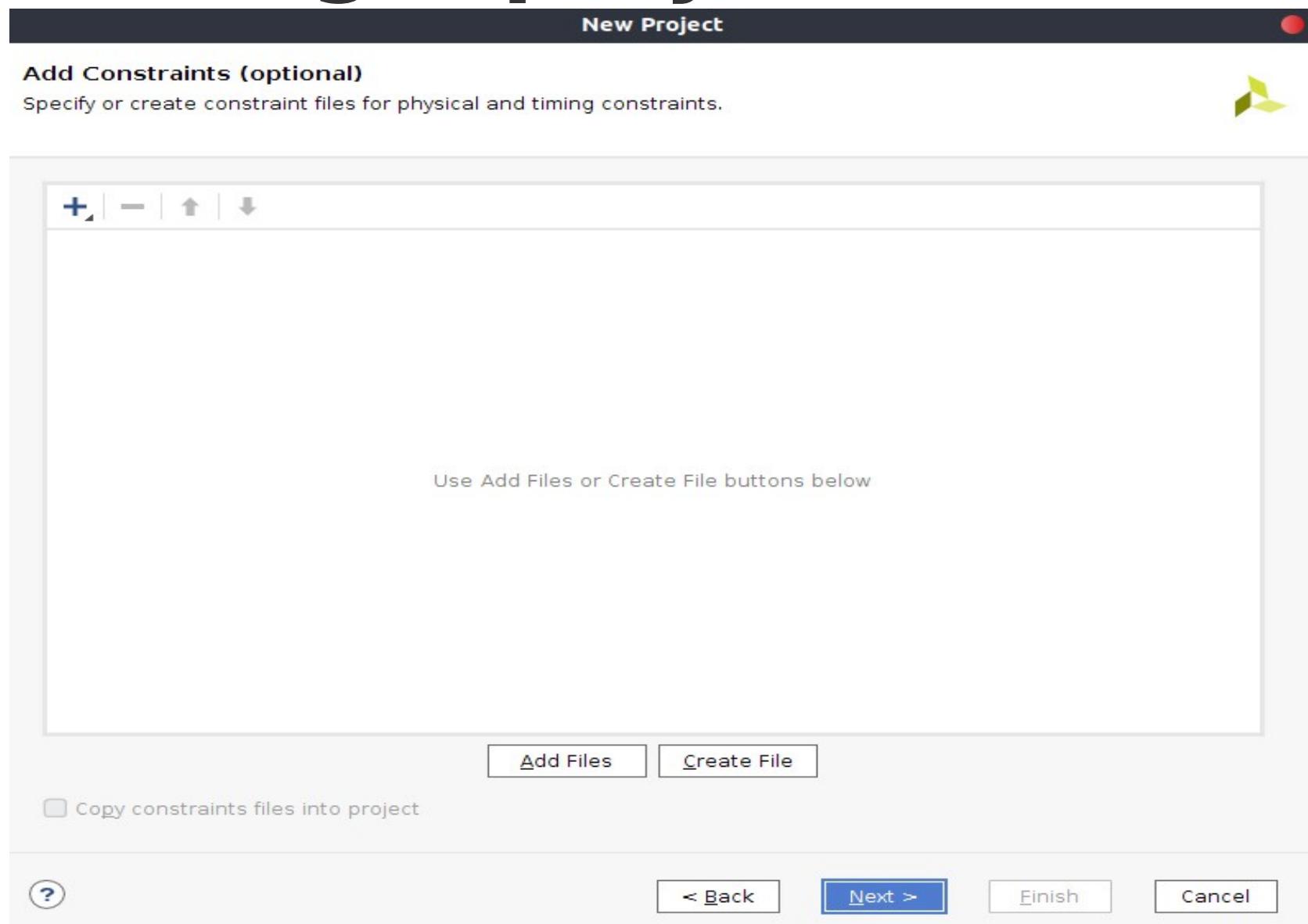
Xilinx Constraints files (XDC)

- FPGAs include some physical pins such as buttons, LEDs, etc.
- If we are planning on using these pins we must inform Vivado to associate them with our HW designs
- All XDC files are provided

Creating a project (cont'd)

New Project

Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.



Use Add Files or Create File buttons below

Copy constraints files into project

[Add Files](#) [Create File](#)

[?](#) [< Back](#) [Next >](#) [Finish](#) [Cancel](#)

Creating a project (cont'd)

New Project

Default Part
Choose a default Xilinx part or board for your project.

Parts | Boards

Reset All Filters

Vendor: em.avnet.c... Name: All Remaining Board Rev: Latest

Search:

Display Name	Preview	Vendor	File Version	Part
ZedBoard Zynq Evaluation and Development Kit Add Daughter Card Connections		em.avnet.com	1.4	xc7z020clg484

?

< Back

Next >

Finish

Cancel



Flow Navigator

- Run Simulation
 - Shows the waveform of the design that represents its behavior
 - Main debugging routine
- Open Elaborated Design
 - Generates and displays the schematic of your design

Flow Navigator

- Run Synthesis
 - Shows the corresponding LUT schematic of the selected device
 - Displays info about timing, utilization and critical paths
- Run Implementation
 - Implements your design and places it on the selected FPGA device

Flow Navigator

- Generate bitstream
 - Generates the bitstream, which is used to program the FPGA
- Open Hardware Manager
 - Finds the connected device
 - Programs Device to download the generated bitstream to the connected device

Work remotely - connect

- Instead of working on your own machine, you can run simulations on Debian machines.
 - Interactively through command line
 - Interactively with GUI through ssh display forwarding (ssh -X <hostname>)

Work remotely - flow

- cp -r ~hy220/tools/example .
- cd example
- source setup.sh
- export HY220_SIMULATOR=[verilator,vivado,icarus]
- Work interactively
 - make
 - make gwaves (after make)
 - It opens the generated wave files with gtkwave viewer

Work remotely - your files

- mkdir project_file
- cp Makefile, setup.sh (from example)
- Edit Makefile (SRCS, TOP_MODULE)
- Repeat compilation flow



Switch to Vivado for demo