Vivado Design Suite

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CS-220
FPGAs

- A field-programmable gate array (FPGA) is a circuit designed to be configured using hardware description language HDL.
Vivado

Produced by Xilinx

• A software suite used for
  1) Simulation
  2) Synthesis

of HDL (Hardware Design Language such as SystemVerilog) designs
Simulation

- The simulation of an electronic circuit helps the HDL programmer by visualizing the circuit’s behavior.
Synthesis

- Synthesis generates LUT-level schematic of the design
Vivado Installation

Vivado Design Suite 2018.3.1 is now available with support for

- Enhancements in the IBERT IP and GT Wizard for Virtex UltraScale+ S6G Devices
- Production devices enabled:
  - Virtex UltraScale+ HBM (-1, -2, -2L): XCVU31P, XCVU33P, XCVU39P, XCVU85P
  - Defense-Grade Zynq UltraScale+ MPSoC Devices: XZU11EG
  - Defense-Grade Kintex UltraScale+ Devices: XU015P, XU05P
  - Defense-Grade Virtex UltraScale+ Devices: XQVU3P
  - Defense-Grade Zynq UltraScale+ RFSoC Devices: XZU29DR

The follow devices are introduced in this release:

- Zynq UltraScale+ RFSoC: XZU39DR
- XA Zynq UltraScale+ MPSoC Devices: XAZU11EG (-1, -1G)

The following devices are introduced in WebPack:

Download Includes: Vivado Design Suite HLx Editions (All Editions)
Last Updated: March 29, 2019
Answers: 2018.3.1 - Vivado Known Issues
Support Forums: Installation and Licensing
Vivado Installation (cont’d)
Welcome

We are glad you’ve chosen Xilinx as your platform development partner. This program can install the Vivado Design Environment, Software Development Kit and Documentation Navigator.

Supported operating systems for Vivado 2018.3 are:
- Windows 7.1: 64-bit
- Windows 10 Professional versions 1803 and 1809: 64-bit
- Red Hat Enterprise Linux 6 6-6.9: 64-bit
- Red Hat Enterprise Linux 7 2.7.5: 64-bit
- CentOS Linux 6 6-6.9: 64-bit
- CentOS Linux 7 2-7.5: 64-bit
- SUSE Enterprise Linux 11.4: 64-bit
- SUSE Enterprise Linux 12.3: 64-bit
- Ubuntu Linux 16.04.4 and 18.04 LTS: 64-bit - Additional library installation required

Note: This release requires upgrading your license server tools to the Flex 11.14.1 versions. Please confirm with your license admin that the correct version of the license server tools are installed and available, before running the tools.

Note: This installation program will not install cable drivers on Linux. This item will need to be installed separately, with administrative privileges.

To reduce installation time, we recommend that you disable any anti-virus software before continuing.
Vivado Installation (cont’d)
Vivado Installation (cont’d)
Vivado Installation (cont’d)

Select Edition to install

Select an edition to continue installation. You will be able to customize the content in the next page.

- **Vivado HL WebPACK**
  Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition. Users can optionally add Model Composer and System Generator for DSP to this installation.

- **Vivado HL Design Edition**
  Vivado HL Design Edition includes the full complement of Vivado Design Suite tools for design, including C-based design with Vivado High-Level Synthesis, implementation, verification and device programming. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add Model Composer to this installation.

- **Vivado HL System Edition**
  Vivado HL System Edition is a superset of Vivado HL Design Edition with the addition of System Generator for DSP. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add Model Composer to this installation.

- **Documentation Navigator (Standalone)**
  Xilinx Documentation Navigator (DocNav) provides access to Xilinx technical documentation both on the Web and on the Desktop. This is a standalone installation without Vivado Design Suite.
Vivado Installation (cont’d)

Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition. Users can optionally add Model Composer and System Generator for DSP to this installation.

- **Design Tools**
  - Vivado Design Suite
    - Vivado
      - System Generator for DSP
      - Model Composer
  - Software Development Kit (SDK)
  - SDK Core Tools
  - Compiler Tool Chains
  - Doceva

- **Devices**
  - Production Devices
    - SoCs
      - Zyq-7000 (limited support)
      - Zynq UltraScale+ MPSoC (limited support)
      - Zynq UltraScale+ MPSoC
    - 7 Series (limited support)
      - Artix-7
      - Kintex-7
      - Spartan-7
      - Virtex-6
    - UltraScale (limited support)
      - Kintex UltraScale
      - Virtex UltraScale
    - UltraScale+ (limited support)
      - Kintex UltraScale+
      - Virtex UltraScale+
      - Virtex UltraScale+ HBM
  - Engineering Sample Devices

- **Installation Options**
  - NOTE: Cable Drivers are not installed on Linux. Please follow the instructions in UG973 to install Linux cable drivers
  - Enable WebTalk for Vivado to send usage statistics to Xilinx (Always enabled for WebPACK license)
  - Enable WebTalk for SDK to send usage statistics to Xilinx

Download Size: 4.63 GB
Disk Space Required: 21.17 GB

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Vivado Installation (cont’d)
### Vivado Installation (cont’d)

**Installation Summary**

**Edition:** Vivado HL WebPACK

- **Devices**
  - Production Devices (SoCs, 7 Series)

- **Design Tools**
  - Vivado Design Suite (Vivado)

- **Installation Options**
  - Enable WebTalk for Vivado to send usage statistics to Xilinx (Always enabled for WebPACK license)

**Installation location**

- `/home/sototo/Vivado/2018.3`

**Download location**

- `/home/sototo/Downloads/Vivado_2018.3`

**Disk Space Required**

- Download Size: 4.63 GB
- Disk Space Required: 21.17 GB

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Creating a project
Creating a project (cont’d)

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

- Project name: test
- Project location: /tools/Xilinx/Vivado/2018.3/bin
- Create project subdirectory

Project will be created at: /tools/Xilinx/Vivado/2018.3/bin/test
Creating a project (cont’d)

Project Type
Specify the type of project to create.

- **BTL Project**
  You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
  - Do not specify sources at this time

- **Post-synthesis Project**: You will be able to add sources, view device resources, run design analysis, planning and implementation.
  - Do not specify sources at this time

- **I/O Planning Project**
  Do not specify design sources. You will be able to view part/package resources.

- **Imported Project**
  Create a Vivado project from a Synplify, XST or ISE Project File.

- **Example Project**
  Create a new Vivado project from a predefined template.
Creating a project (cont’d)

Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Use Add Files, Add Directories or Create File buttons below

- Add Files
- Add Directories
- Create File

Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories

Target language: Verilog
Simulator language: Mixed

< Back  Next >  Finish  Cancel
Create a project (cont’d)
Create a project (cont’d)

Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.

Use Add Files or Create File buttons below

☐ Copy constraints files into project

< Back  Next >  Finish  Cancel
Constraints file

- When programming an FPGA through software such as Xilinx’s Vivado, you need to inform the software what physical pins on the FPGA that you plan on using.
- Xilinx Design Constraints file (XDC file)
Creating a project (cont’d)
Flow Navigator

- Run Simulation
  - Will show the waveform of the design that represents its behavior
    → most bugs can be caught here!!!

- Open Elaborated Design
  - Generates the schematic of your code
    → can be useful when you want to know exactly all and non-trivial connections of the design
Flow Navigator

- Run Synthesis
  - Will show the corresponding LUT schematic of the selected device
    → Info about timing, utilization and critical paths!!!

- Run Implementation
  - Here the same schematic as before will be showed with the design implemented on it for our selected device
Flow Navigator

- Generate Bitstream
  - In here the bitstream is generated by the initial design in order to program the selected device

- Open Hardware Manager
  - Open Target to find the connected device
  - Program Device to download the generated bitstream to the connected device!
Demo time!!!

Questions...?