HY - 220

Introduction to Vivado and isim simulator

Xirouchakis Pantelis

Vivado Installation

- Vivado HL System Edition

- Documentation Navigator (Standalone)

The Web Installer will accept your login credentials and allow you to select the edition, device families and tool components (SDK or DocNav). It will then automatically download only your selection and install it on your local machine.

Note: Use the Web Installers to install Vivado HL WebPACK and cut your download time by up to 2/3 and download size by up to 6GB!

For more information, please watch the Installation Overview Video.

Please be aware that with the release of version 2016.2, DVDs and any other forms of downloadable physical shipment will no longer be available for ordering and will only be available for download at Xilinx.com.

Vivado HLx 2017.1: WebPACK and Editions - Windows Self Extracting Web Installer (EXE - 51.5[illegible] MB)
MD5 SUM Value: df4c2611b3fd[illegible]db8c8f184bf7ee5bbba

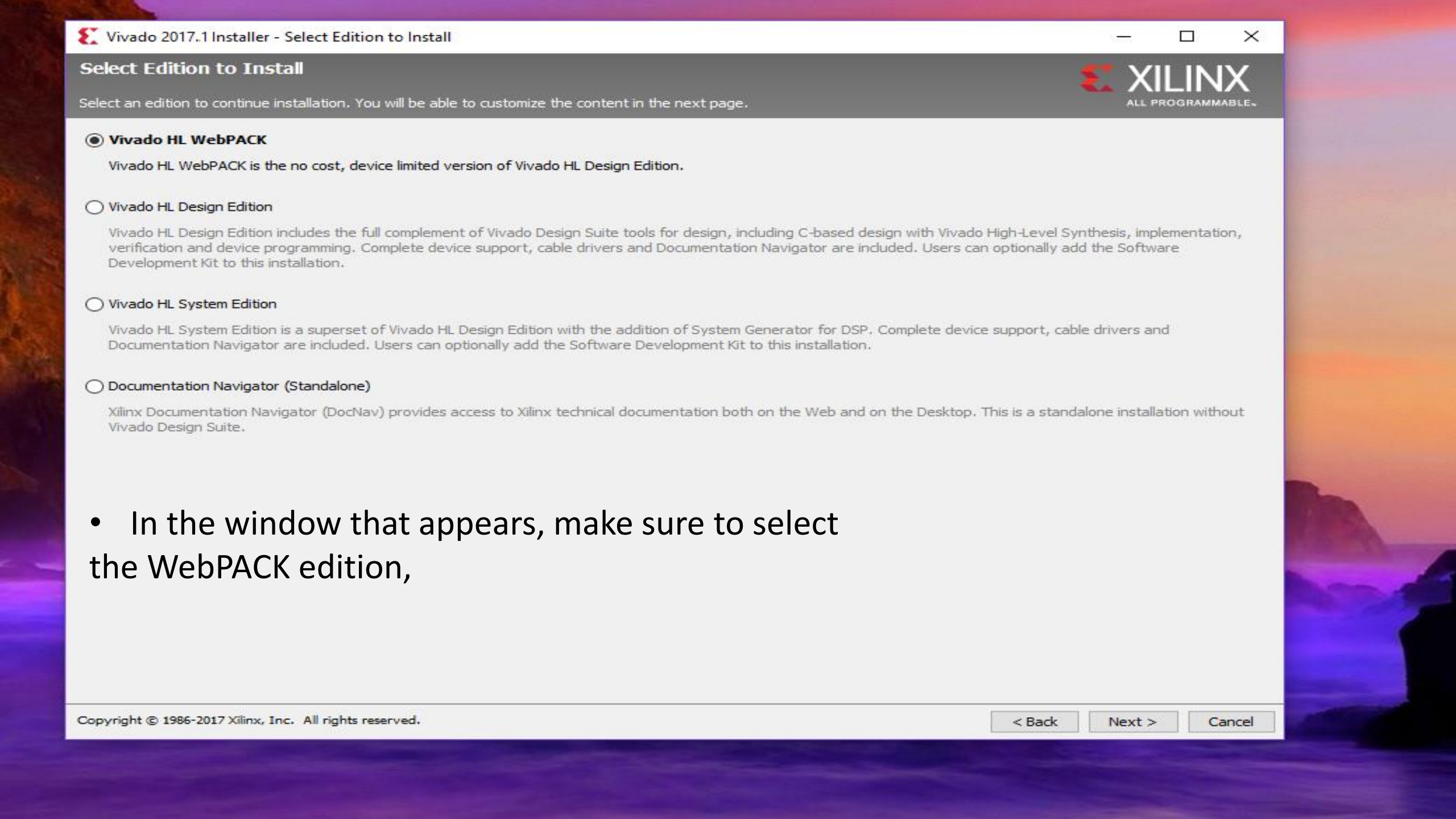
Vivado HLx 2017.1: WebPACK and Editions - Linux Self Extracting Web Installer (BIN - 85.23 MB)
MD5 SUM Value: 42fd14f5472de77a54ba1f847c00eec2

Vivado HLx 2017.1: All OS installer Single-File Download (TAR/GZIP - 20.21 GB)
MD5 SUM Value: ee351905f061e19751999e69b41f4b22

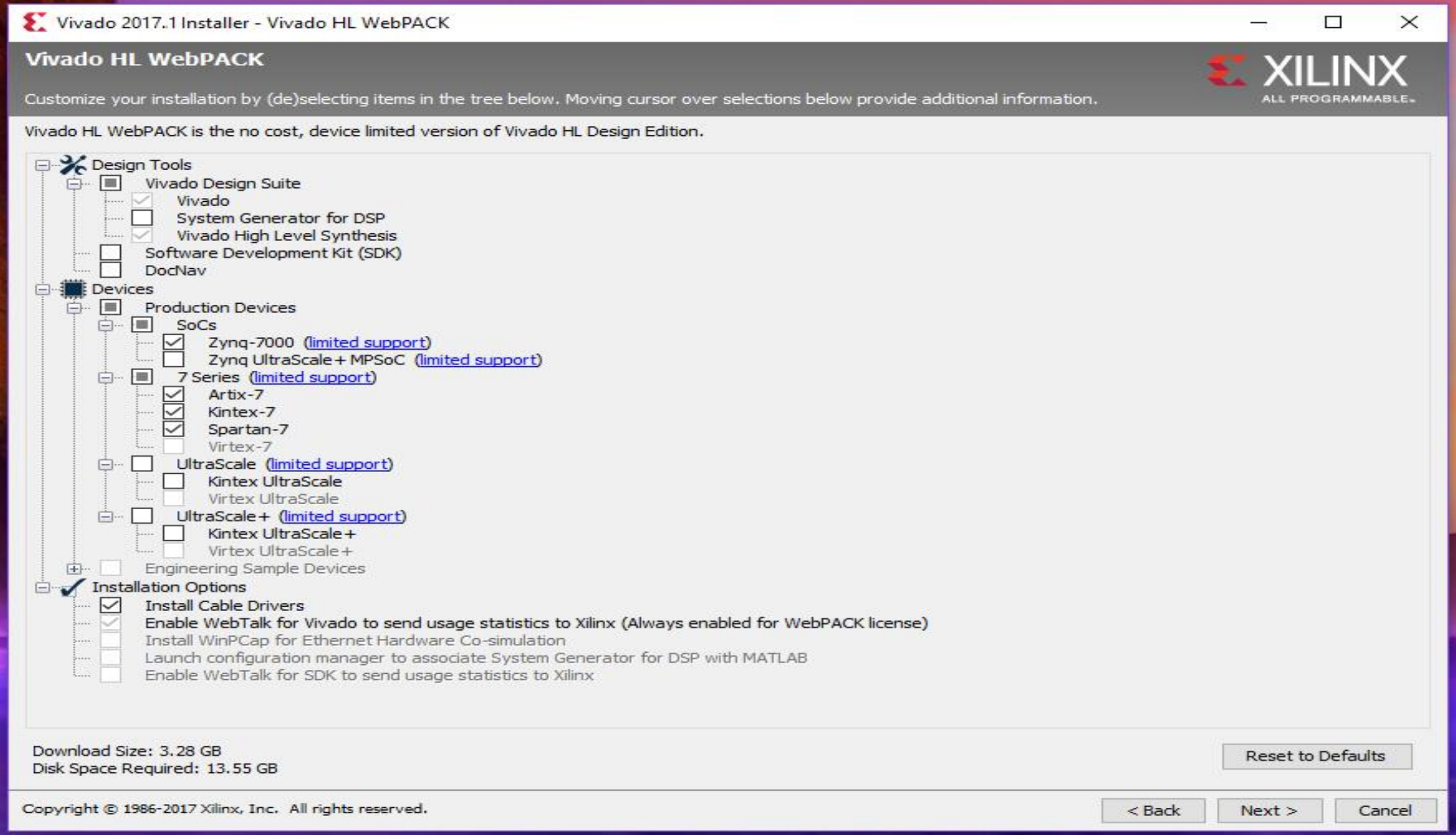
Navigate to the Xilinx Downloads page, and Download Vivado 2017.1 WebPack edition.

We are going to use version 2017.1 , but any other Vivado version will do.

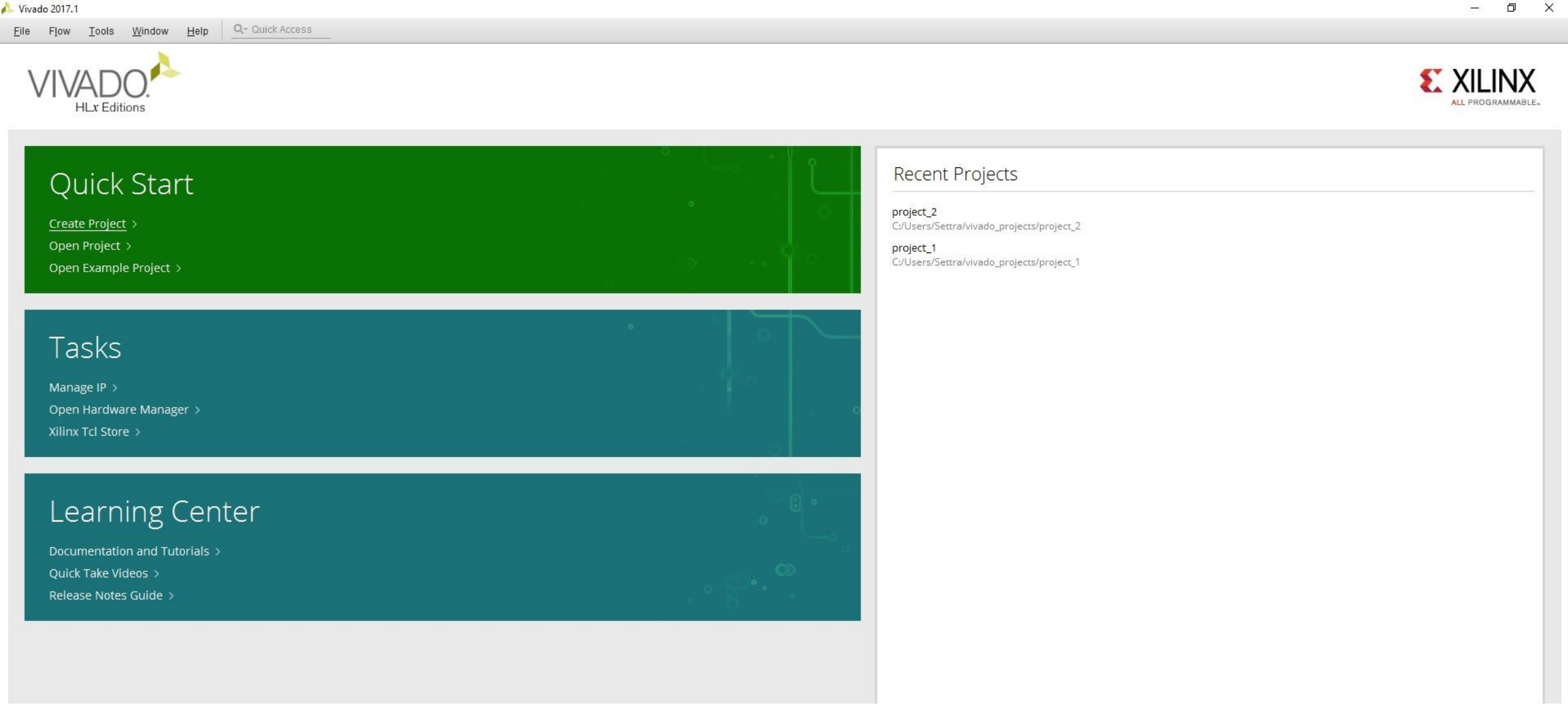
Use the Web Installer, in order to minimize The required download space.



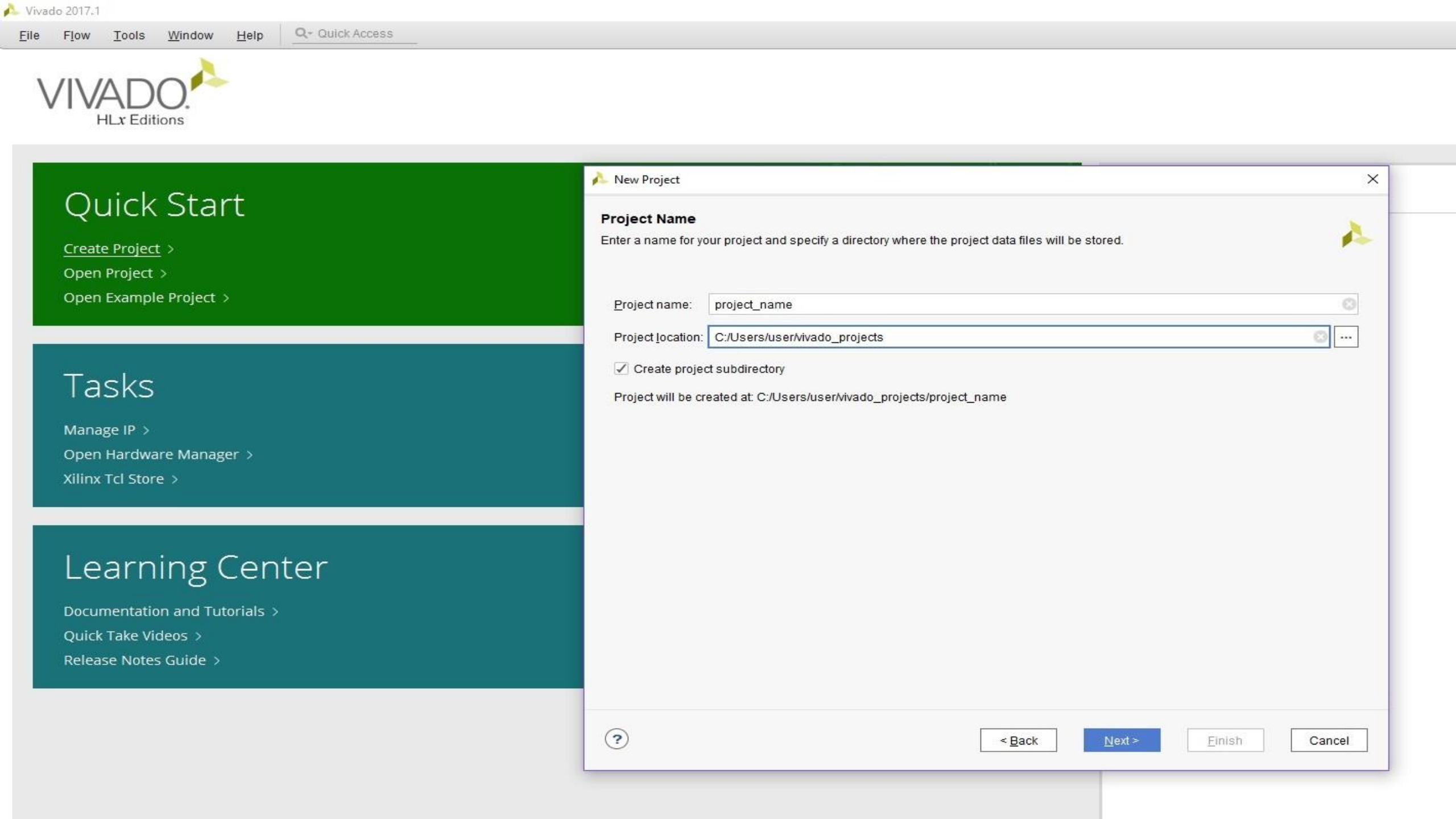
- In the window that appears, make sure to select the WebPACK edition,

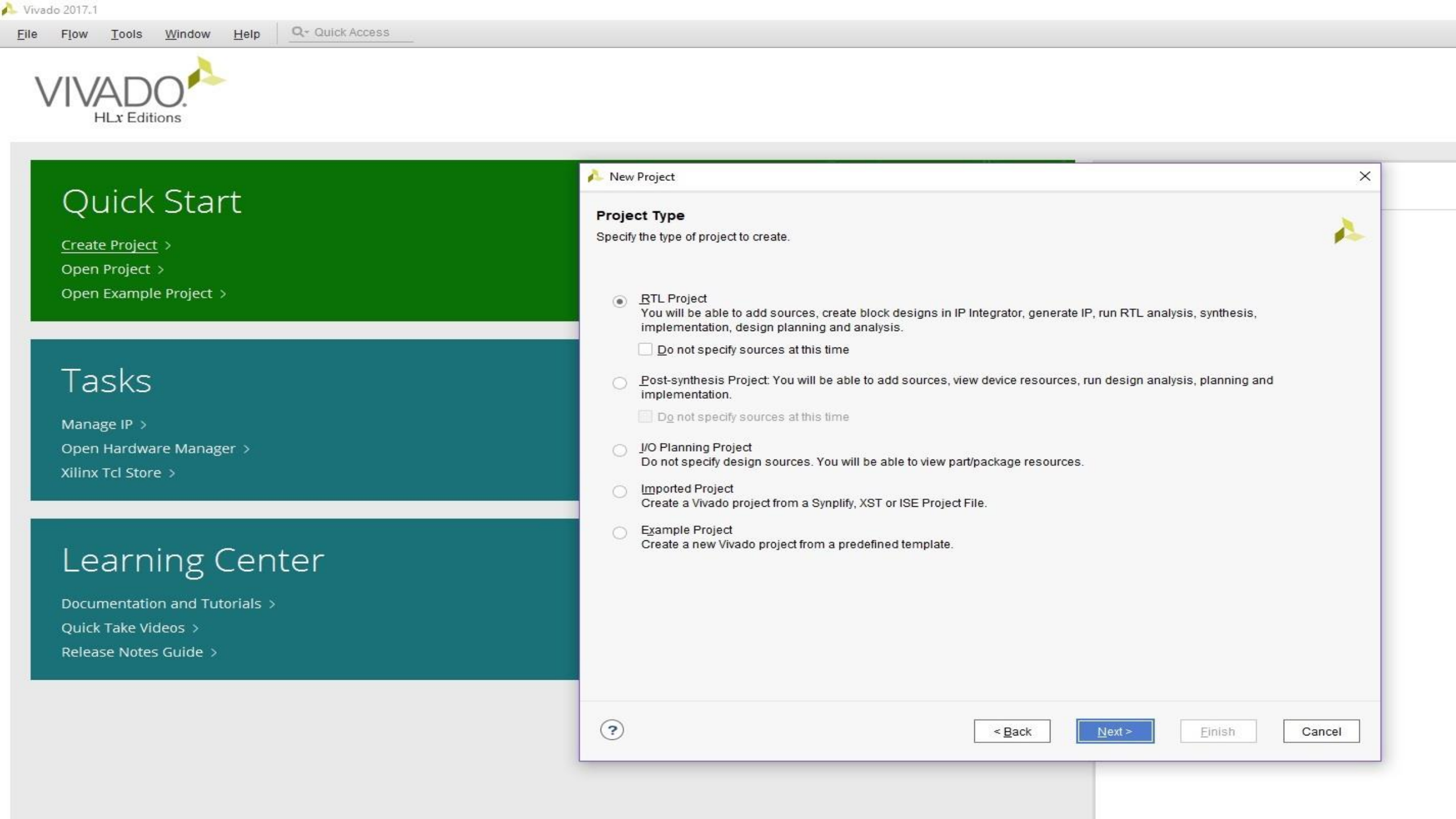

Vivado 2017.1 Installer - Vivado HL WebPACK
Vivado HL WebPACK
Customize your installation by (de)selecting items in the tree below. Moving cursor over selections below provide additional information.
XILINX
ALL PROGRAMMABLE.
Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition.
Design Tools
Vivado Design Suite
Vivado
System Generator for DSP
Vivado High Level Synthesis
Software Development Kit (SDK)
DocNav
Devices
Production Devices
SoCs
Zynq-7000 (limited support)
Zynq UltraScale+ MPSoC (limited support)
7 Series (limited support)
Artix-7
Kintex-7
Spartan-7
Virtex-7
UltraScale (limited support)
Kintex UltraScale
Virtex UltraScale
UltraScale+ (limited support)
Kintex UltraScale+
Virtex UltraScale+
Engineering Sample Devices
Installation Options
Install Cable Drivers
Enable WebTalk for Vivado to send usage statistics to Xilinx (Always enabled for WebPACK license)
Install WinPCap for Ethernet Hardware Co-simulation
Launch configuration manager to associate System Generator for DSP with MATLAB
Enable WebTalk for SDK to send usage statistics to Xilinx
Download Size: 3.28 GB
Disk Space Required: 13.55 GB
Reset to Defaults
Copyright © 1986-2017 Xilinx, Inc. All rights reserved.
< Back
Next >
Cancel

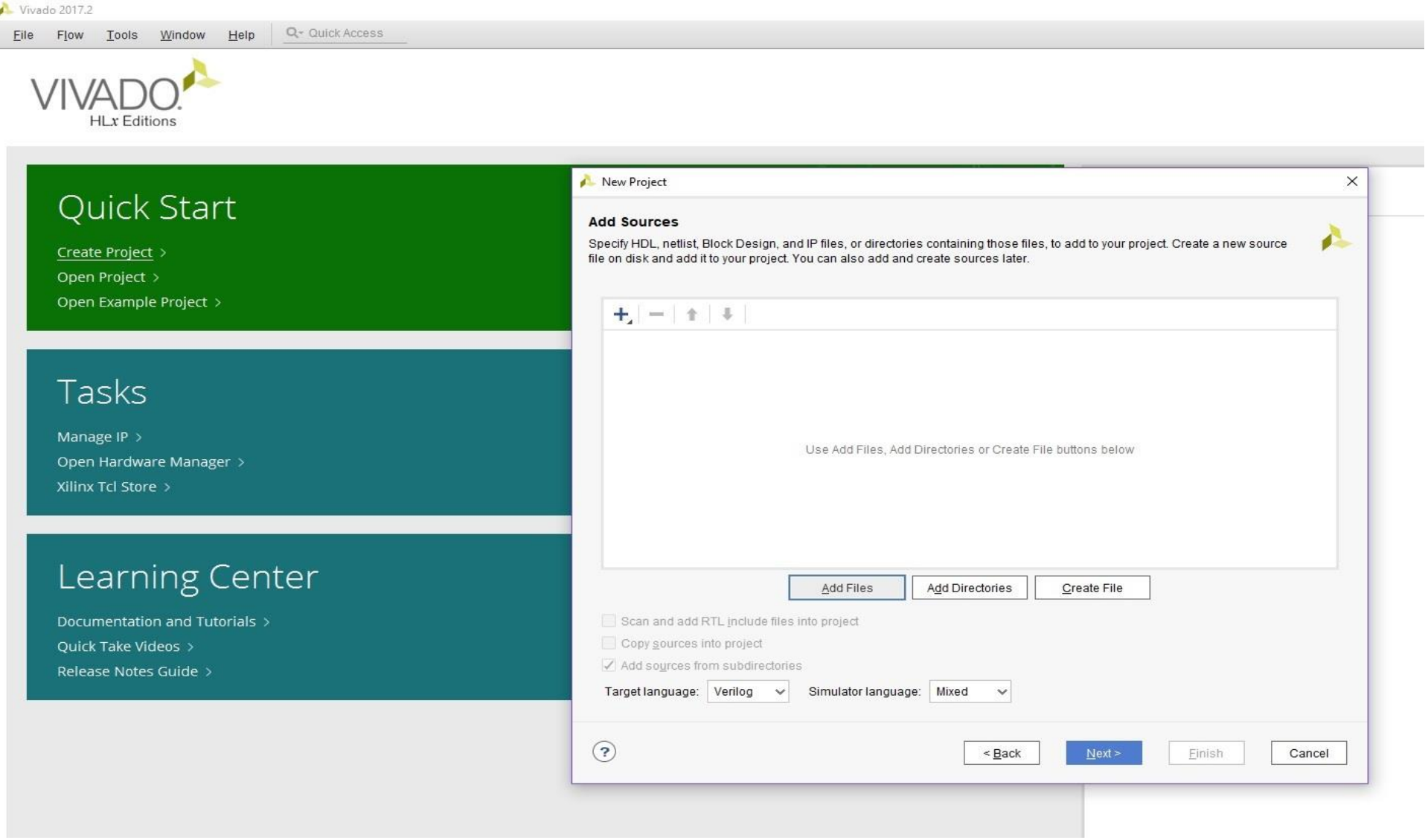
Creating a new Project



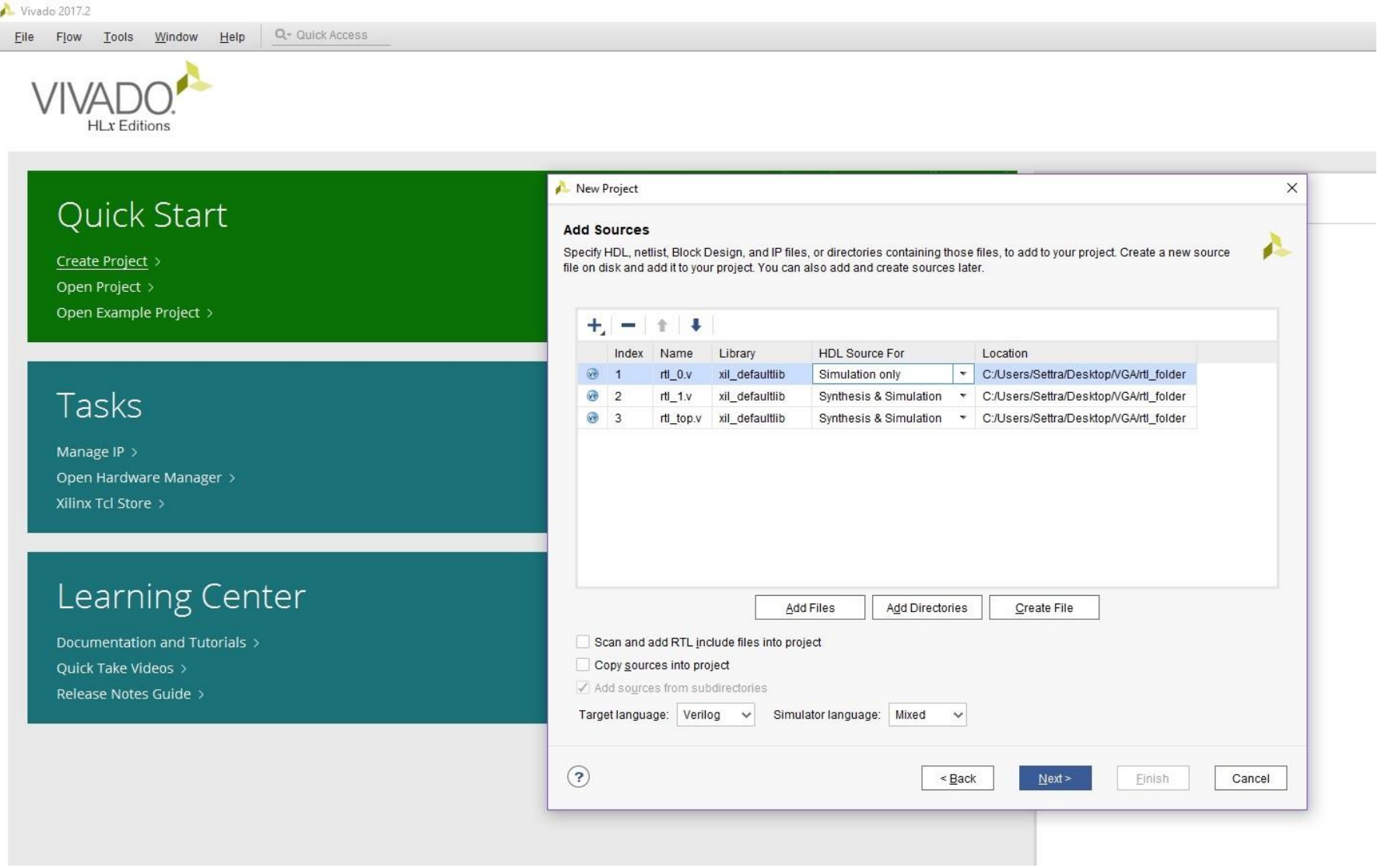
- When you run Vivado, this is the window that appears. Select “create project”


Vivado 2017.1
File
Flow
Tools
Window
Help
Quick Access
VIVADO
HLx Editions
Quick Start
Create Project >
Open Project >
Open Example Project >
Tasks
Manage IP >
Open Hardware Manager >
Xilinx Tcl Store >
Learning Center
Documentation and Tutorials >
Quick Take Videos >
Release Notes Guide >
New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
project_name
Project location:
C:/Users/user/vivado_projects
Create project subdirectory
Project will be created at: C:/Users/user/vivado_projects/project_name
< Back
Next >
Finish
Cancel

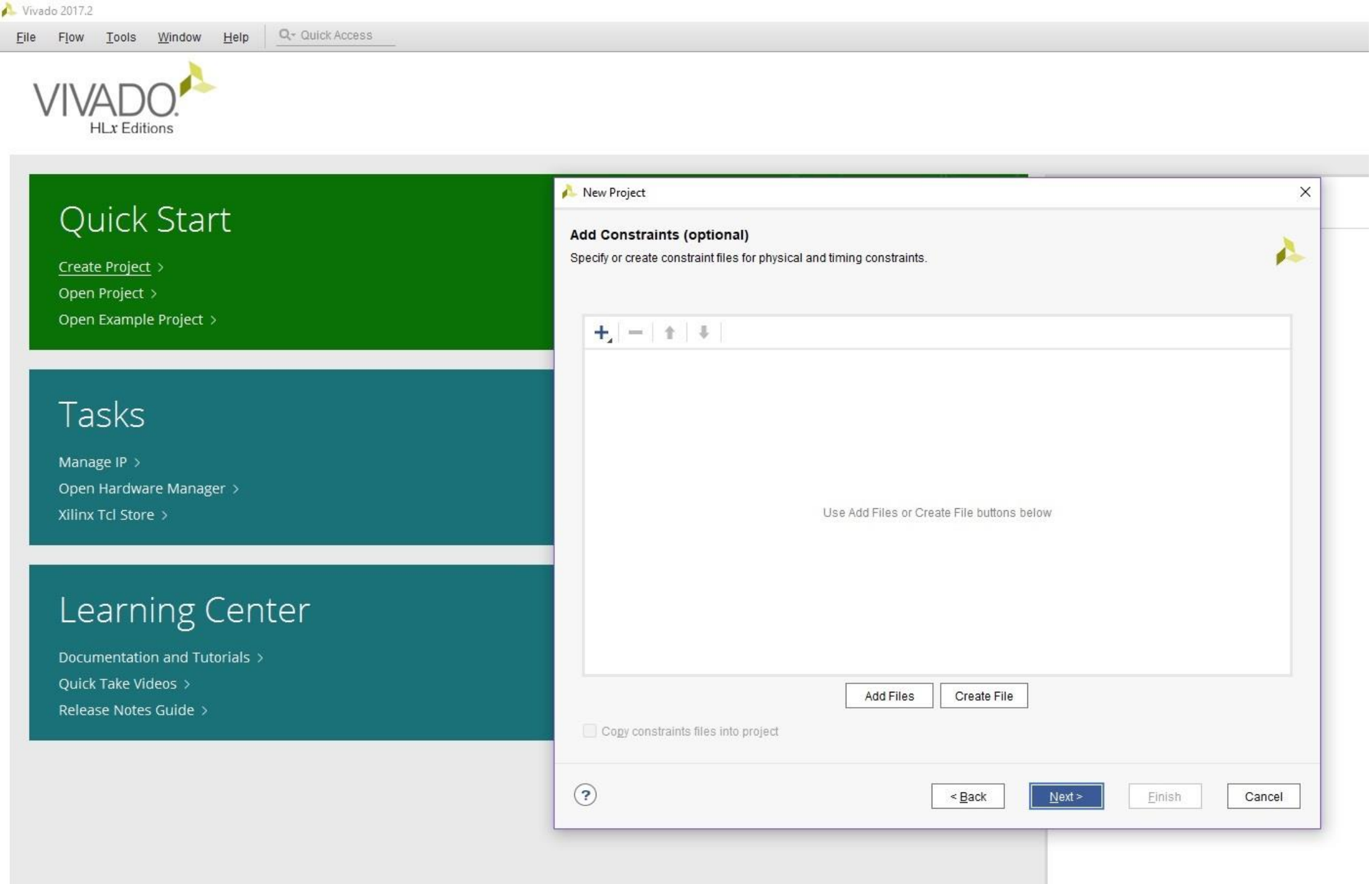

Vivado 2017.1
File
Flow
Tools
Window
Help
Quick Access
VIVADO
HLx Editions
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
Xilinx Tcl Store
Learning Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel



- If you have your code ready, you can add it by selecting “add files”.
- You can always add more files later



- Files used for simulation should be set as “simulation only” in the drop down menu. All others as “synthesis & simulation”
- Selecting “Copy sources into project” will copy the source files, into the project subdirectory. Warning: Any changes made to them, when opening the files from Vivado, will happen to the copied sources, and not in the original location.


Vivado 2017.2
File
Flow
Tools
Window
Help
Quick Access
VIVADO
HLx Editions
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
Xilinx Tcl Store
Learning Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

Vivado 2017.2

File Flow Tools Window Help Quick Access

VIVADO HLx Editions

Quick Start

Create Project >
Open Project >
Open Example Project >

Tasks

Manage IP >
Open Hardware Manager >
Xilinx Tcl Store >

Learning Center

Documentation and Tutorials >
Quick Take Videos >
Release Notes Guide >

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: Parts Boards

Filter/ Preview

Vendor: em.avnet.com

Display Name: ZedBoard Zynq Eval...

Board Rev: Latest

Reset All Filters

Search:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484	1.3

No Board Connectors

< Back Next > Finish Cancel

Next Page

File Edit Flow Tools Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

PROJECT MANAGER - project_name

Sources

- Design Sources (1)
  - **adder_top** (adder_top.v) (4)
    - FA_0 : full_adder (full_adder.v) (2)
    - FA_1 : full_adder (full_adder.v) (2)
    - FA_2 : full_adder (full_adder.v) (2)
    - FA_3 : full_adder (full_adder.v) (2)
- Constraints
  - constrs_1
- Simulation Sources (1)
  - sim_1 (1)
    - **tb** (adder_tb.v) (1)
      - UUT : adder_top (adder_top.v) (4)
        - FA_0 : full_adder (full_adder.v) (2)
        - FA_1 : full_adder (full_adder.v) (2)
        - FA_2 : full_adder (full_adder.v) (2)
        - FA_3 : full_adder (full_adder.v) (2)

Hierarchy Libraries Compile Order

Source File Properties

adder_tb.v

General Properties

Project Summary

Settings Edit

Project name:	project_name
Project location:	C:/Users/Settra/vivado_projects/project_name
Product family:	Zynq-7000
Project part:	ZedBoard Zynq Evaluation and Development Kit (xc7z020clg484-1)
Top module name:	adder_top
Target language:	Verilog
Simulator language:	Mixed

Board Part

Display name:	ZedBoard Zynq Evaluation and Development Kit
Board part name:	em.avnet.com:zed:part0:1.3
Connectors:	
Repository path:	C:/Xilinx/Vivado/2017.2/data/boards/board_files
URL:	http://www.zedboard.org
Board overview:	ZedBoard Zynq Evaluation and Development Kit

Synthesis

Status:	Not started
Messages:	No errors or warnings
Part:	xc7z020clg484-1

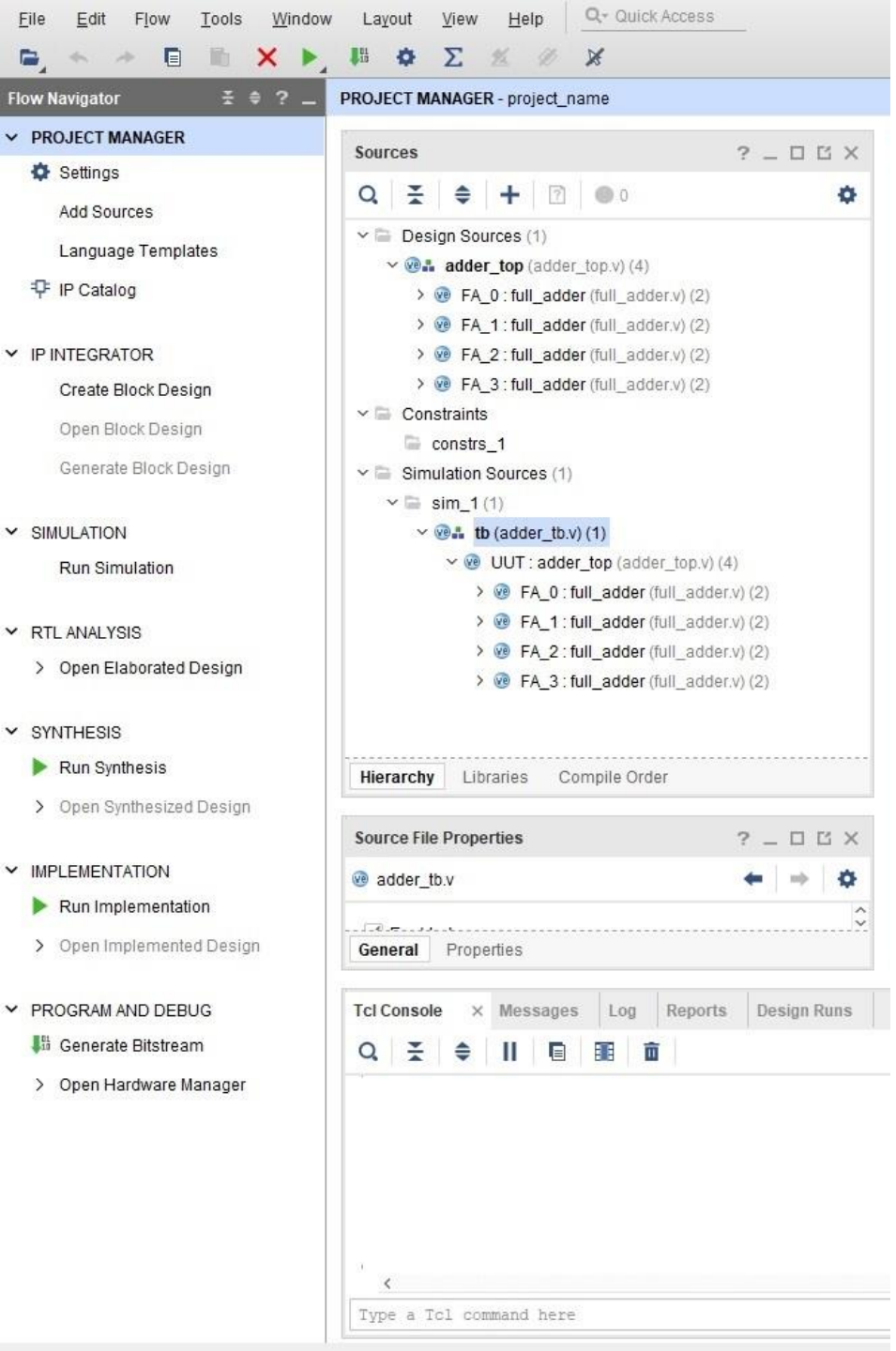
Implementation

Status:	Not started
Messages:	No errors or warnings
Part:	xc7z020clg484-1

Tcl Console | Messages | Log | Reports | Design Runs

Type a Tcl command here

- **Flow Navigator**. From here you can :
  - Add a new IP
  - Elaborate the design
  - Synthesize and Implement the design
  - Open Hardware manager, to download the bitstream in the FPGA.
- **Elaborate design.** Gives the main idea, of the schematic, that the tool (Vivado) understands by your code.
  - Helps supervise non-trivial connections (i.e generated by a generate block)
  - Especially usefull when trying to solve “multi-driven” error issues
- **Synthesize design.** Generates the LUT-level schematic of the design. From here you can check timing , utilization, and critical paths.
- **Implement design.** Implements the synthesized design, to the FPGA device that we are using.



From the sources window, we are going to use only the "Hierarchy" tab. It consists of:

- Design sources: the actual code of our module.
- Simulation sources: Code only used for the simulation of our module i.e testbench.
- Constraints: .xdc files used for synthesis/implementation. These files contain information on how the I/O of our module, connects to actual I/O of the FPGA. It also has information about the clock, used by the tool to synthesize the design accordingly.

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
    - Report Methodology
    - Report DRC
    - Report Noise
    - Schematic
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

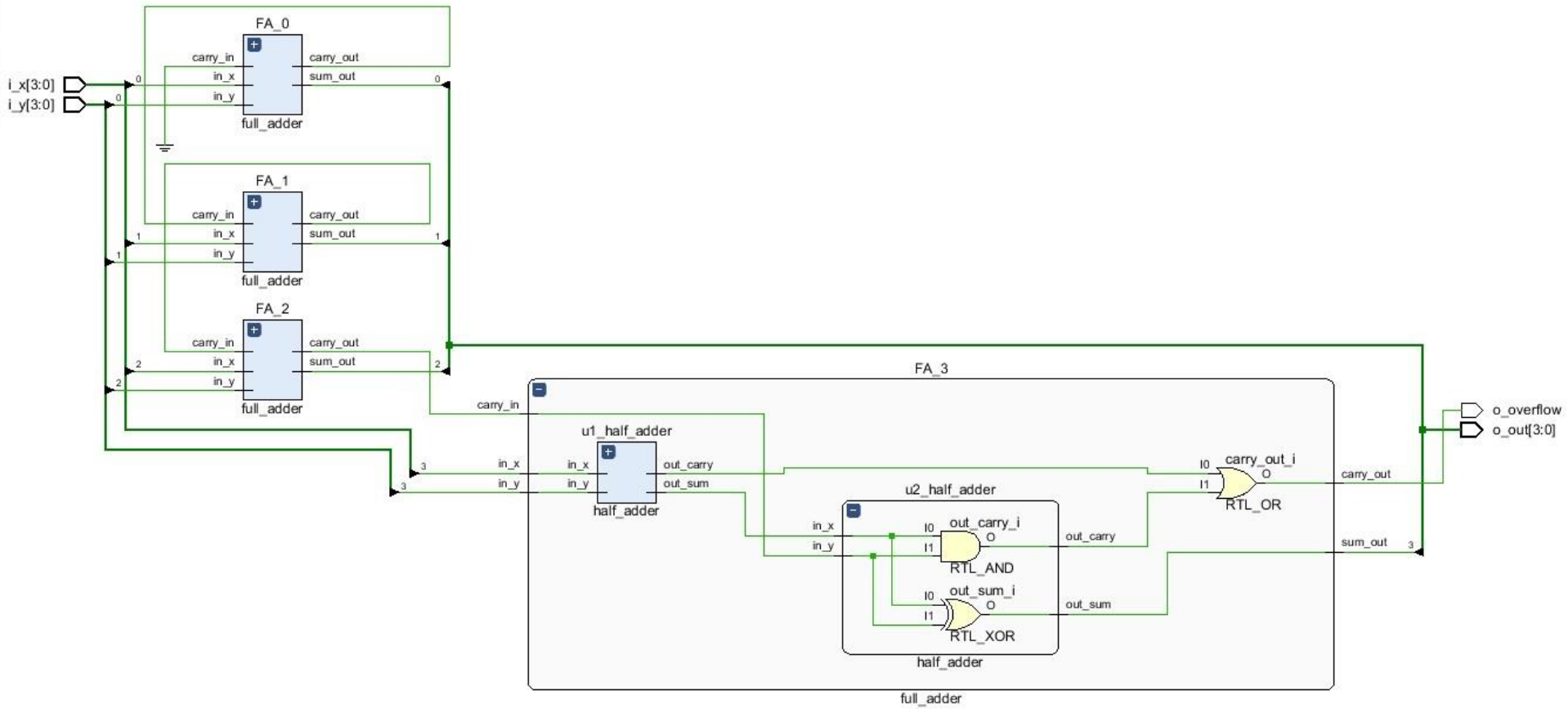
ELABORATED DESIGN - xc7z020clg484-1 (active)

Cell Properties | Sources | Netlist

Project Summary | Schematic | adder_top.v | adder_tb.v

9 Cells 13 I/O Ports 29 Nets

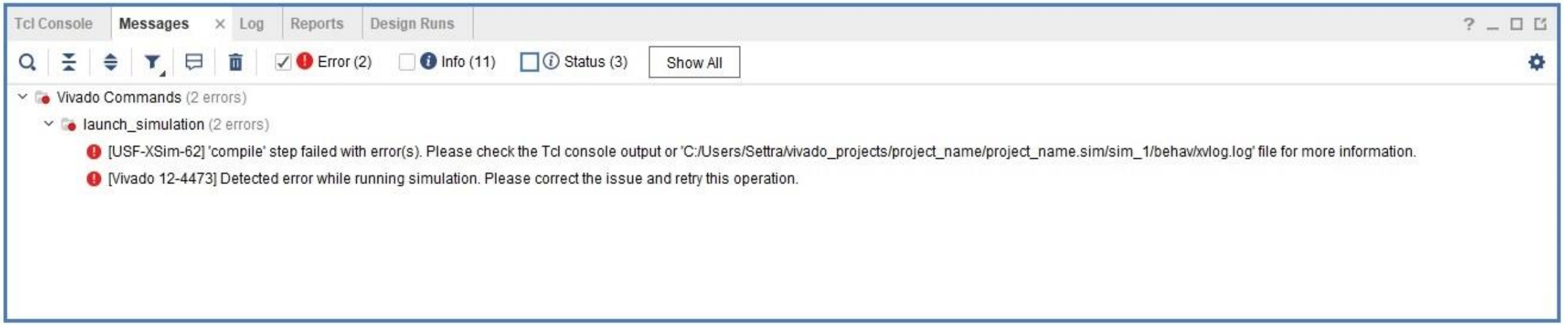
Elaborated design example, of a 4-bit adder



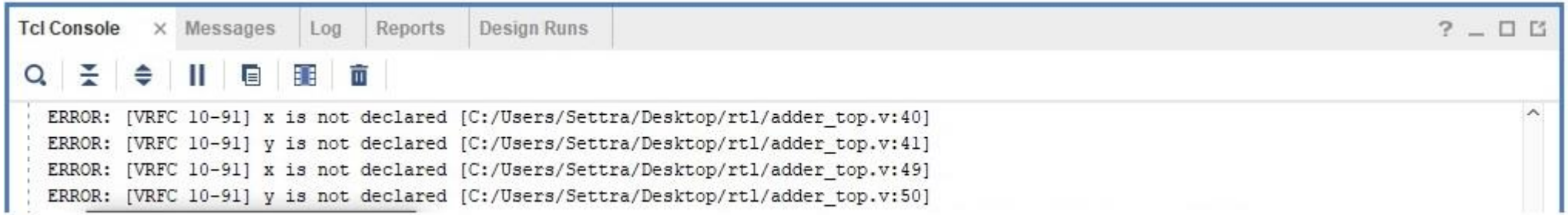
Tcl Console | Messages | Log | Reports | Design Runs

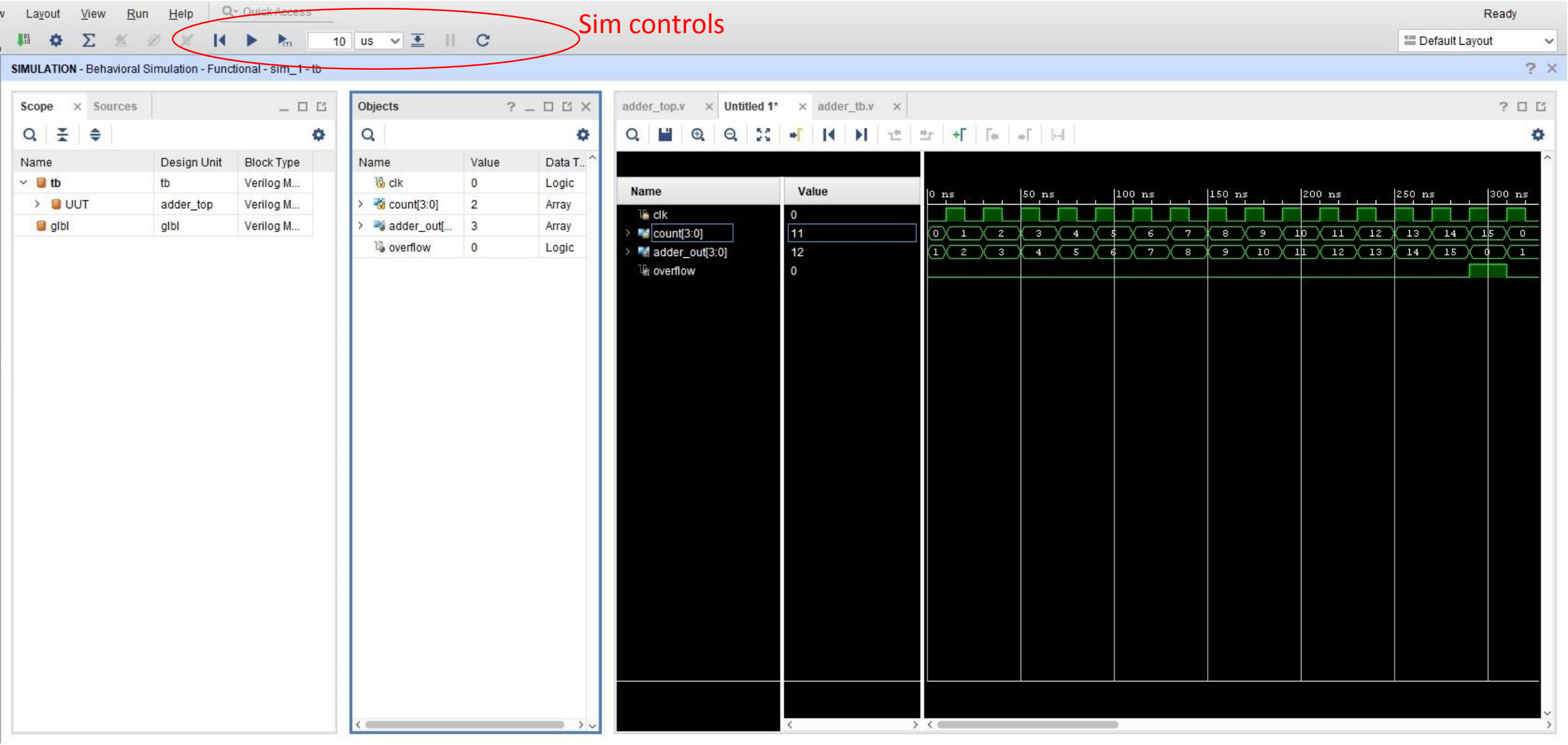
Simulation

- Click “Run Simulation” -> “Run behavioral Simulation”
- Usually, if errors occur, you will get messages like that:



If that’s the case, more details about the errors can be found in the “Tcl console” tab



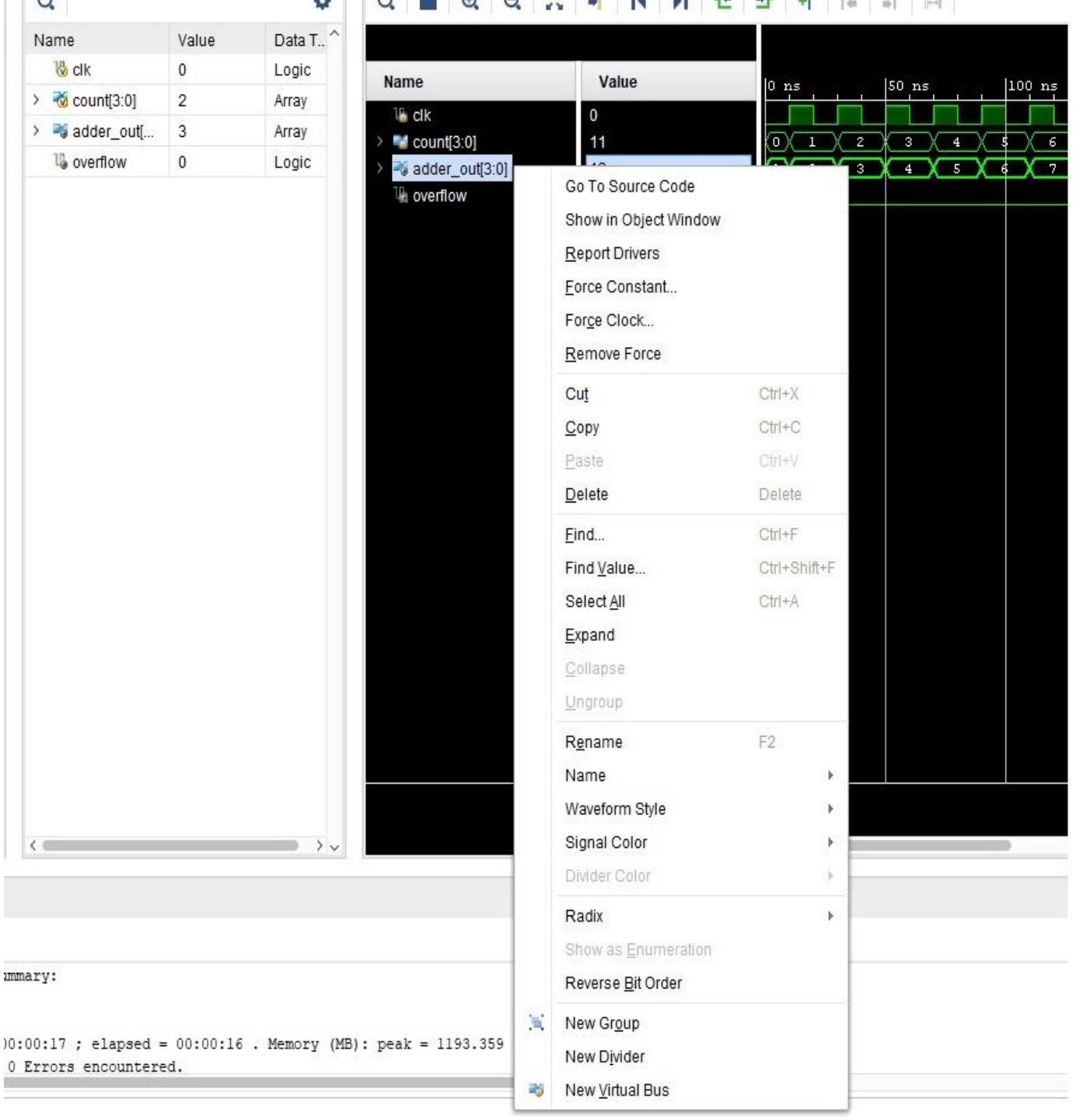


If all went well, you should get a screen like that

- **Sim controls**: reset simulation, or move forward in time. Or relaunch simulation, if source files have changed.

- **Scope**: All the instantiated modules found in your Verilog code.

- **Objects**: all the “variables” , of the module selected in the “scope” window. Wires, registers, IO. From here you can drag and drop them in the simulation window in order to monitor them.



By right clicking on a signal you can:

- **Force a constant value**: Force the signal to act as having a specific value, usually to see how other signals will react. Be sure to do it AFTER the simulation has been reset.
- **Radix**: Choose if the values are represented in hex/dec etc.
- **Signal Color**: change the waveform color of the signal. Useful for grouping signals. Just avoid orange, blue and red since simulator already uses those.
- **New divider**: add a divider line between signals, for easier grouping.
- **New virtual Bus**: usually useful for splitting larger busses, into smaller ones, with meaningful values