Queue and Flow Control Architectures for Interconnection Switches

- 1. Basic Concepts and Queueing Architectures
- 2. High-Throughput Multi-Queue Memories
- 3. Crossbars, Scheduling, & Combination Queueing
- 4. Flow and Congestion Control in Switching Fabrics

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4.1 Parallelism for High-Thruput: Inverse Multiplexing				
Bit	Byte-Slice	Packet	Flow	
bit 1 of 8	By. 1-8	packet 1	flow 1	
bit 2 of 8	By. 9-16	packet 2	flow 2	
bit 3 of 8	By. 17-24	packet 3	flow 3	
bit 4 of 8	By. 25-32	packet 4	flow 4	
bit 5 of 8	By. 33-40	packet 5	flow 5	
bit 6 of 8	By. 41-48	packet 6	flow 6	
bit 7 of 8	By. 49-56	packet 7	flow 7	
bit 8 of 8	By. 57-64	packet 8	flow 8	
- 、	of 64B cell Inve		verse Multiplexing	
same handling for all wires different handling				
(same time, same destination) (diff. times & destinations)				
 Parallel wires or network routes for scaling (virtual) "link" throughput up Easy: central control, synchronized; Difficult: distributed control, asynch. 				
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Per-Flow Inverse Muxing for Non-Blocking Operation • Prove that overall N×N network is non-blocking, i.e. any feasible external traffic \Rightarrow feasible rates on all internal links · All traffic entering switch A is feasible, hence of aggregate rate \leq 1+1 = 2; it is split into two halves \Rightarrow each of rate \leq 1 \Rightarrow traffic entering each (N/2)×(N/2) subnetwork is feasible • It does not suffice to balance (equalize) the aggregate load out of switch A - must equally distribute individual (end-toend) flows - per-flow inverse multiplexing \Rightarrow each of $\lambda_{2,i}$; $\lambda_{3,i}$; $\lambda_{6,i}$ is individually split in two equal halves \Rightarrow the sum of $\lambda_{3,i}$ + $\lambda_{6,i}$ is also split in two equal halves • All traffic exiting switch D is feasible, hence of aggregate rate \leq 1+1 = 2; it enters D in two equal halves \Rightarrow each of rate \leq 1 \Rightarrow traffic exiting each (N/2)×(N/2) subnetwork is also feasible 8 4.1 - M. Katevenis, FORTH and U.Crete, Greece

















































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