Static Random Access Memory
Overview

• Memory is a collection of storage cells with associated input and output circuitry
  Possible to read and write cells
• Random access memory (RAM) contains words of information
• Data accessed using a sequence of signals
  Leads to timing waveforms
• Decoders are an important part of memories
  Selects specific data in the RAM
• Static RAM loses values when circuit power is removed.
Comments about Memory Access and Timing

- Most computers have a central processing unit (CPU)
  - Processor generates control signals, address, and data
  - Values stored and then read from RAM

- The timing of the system is very important.
  - Processor provides data for the cycle time on writes
  - Processor waits for the access time for reads
Memory Arrays

Random Access Memory

Read/Write Memory (RAM) (Volatile)
  - Static RAM (SRAM)
  - Dynamic RAM (DRAM)

Read Only Memory (ROM) (Nonvolatile)
  - Serial In Parallel Out (SIPO)
  - Parallel In Serial Out (PISO)

Serial Access Memory

Serial Access Memory

Content Addressable Memory (CAM)

Shift Registers

Queues

First In First Out (FIFO)

Last In First Out (LIFO)

Mask ROM

Programmable ROM (PROM)

Erasable Programmable ROM (EPROM)

Electrically Erasable Programmable ROM (EEPROM)

Flash ROM
Types of Random Access Memories

- **Static random access memory (SRAM)**
  - Operates like a collection of latches
  - Once value is written, it is guaranteed to remain in the memory as long as power is applied
  - Generally expensive
  - Used *inside* processors (like the Pentium)

- **Dynamic random access memory (DRAM)**
  - Generally, simpler internal design than SRAM
  - Requires data to be rewritten (refreshed), otherwise data is lost
  - Often hold larger amount of data than SRAM
  - Longer access times than SRAM
  - Used as *main memory* in computer systems
Δύο Κατηγορίες Μνήμης

**Static RAM (SRAM)**

Δεδομένα αποθηκεύονται σε Latch.

- Ταχύτερη προσπέλαση μνήμης.
- Δεν χρειάζεται refreshing.
- Καλή συμπεριφόρα στον θόρυβο.
- Μεγαλύτερο μέγεθος από DRAM.

**Dynamic RAM (DRAM)**

Δεδομένα αποθηκεύονται σε φορτίο dynamic node.

- Μικρό μέγεθος μνήμης.
- Χρειάζεται refreshing λόγω leakage. Πιο αργή από SRAM.
- Προβλήματα με θόρυβο (noise).

write/read

data

storage cell

write/read

data

C

storage cell
RAM Interface Signals

- Data input and output lines carry data
- Memory contains $2^k$ words
  - $k$ address lines select one word out of $2^k$
- Read asserted when data to be transferred to output
- Write asserted when data input to be stored

Fig. 7-2 Block Diagram of a Memory Unit
Random Access Memory Fundamentals

- Lets consider a simple RAM chip
  - 8 words of 2 bytes each (each word is 16 bits)
  - How many address bits do we need?

<table>
<thead>
<tr>
<th>Dec</th>
<th>Binary</th>
<th>16 Data and Input signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>000</td>
<td>01010000 11100110</td>
</tr>
<tr>
<td>1</td>
<td>001</td>
<td>11001100 11111111</td>
</tr>
<tr>
<td>2</td>
<td>010</td>
<td>00000000 10101010</td>
</tr>
<tr>
<td>3</td>
<td>011</td>
<td>01010110 00111111</td>
</tr>
<tr>
<td>4</td>
<td>100</td>
<td>11111111 00000000</td>
</tr>
<tr>
<td>5</td>
<td>101</td>
<td>00000001 10000000</td>
</tr>
<tr>
<td>6</td>
<td>110</td>
<td>01010101 11001100</td>
</tr>
<tr>
<td>7</td>
<td>111</td>
<td>00000000 11111111</td>
</tr>
</tbody>
</table>

Pick one of 8 locations

Each bit stored in a binary cell
Αρχιτεκτονική Μνήμης

Row Decoder
Row Address

Storage cell
Word line

Bit line

Sense amplifiers(read)/Drivers (write)

Column decoder
Column Address

Data I/O

Read: select desired bits
Write: do not write unwanted bit
Inside the RAM Device

- Address inputs go into decoder
  - Only one output active
- Word line selects a row of bits (word)
- Data passes through OR gate
- Each binary cell (BC) stores one bit
- Input data stored if Read/Write is 0
- Output data driven if Read/Write is 1

Fig. 7-6 Diagram of a $4 \times 4$ RAM
Inside the SRAM Device

- Note: delay primarily depends on the number of words
- Delay not effected by size of words

° How many address bits would I need for 16 words?
Array Architecture

- $2^n$ words of $2^m$ bits each
- If $n \gg m$, fold by $2^k$ into fewer rows of more columns

- Good regularity – easy to design
- Very high density if good cells are used
Six transistor CMOS SRAM cell.

When the word line is energized (V\textsubscript{DD}), the value of the Latch reads at the bit and bit at the reading of the memory or the value of the Latch is written from the bit and bit at the writing of the memory.
SRAM Banks
Read Operation

CLOCK

ADSP

ADSC

ADDRESS

WRITE

CS

ADV

OE

Data Out

BURST CONTINUED WITH NEW BASE ADDRESS

Q1-1 Q2-1 Q2-2 Q2-3 Q2-4 Q3-1 Q3-2 Q3-3 Q3-4
Write Operation

The diagram illustrates the timing and logic levels for a write operation, with various signals and timing notations such as clock (CLOCK), address (ADDRESS), write (WRITE), chip select (CS), address/data valid (ADV), output enable (OE), data in (Data In), and data out (Data Out). Specific signals and timing markers like tss, th, tcv, tc, tsh, and ts are also shown to detail the operation's sequence and timing parameters.
Example 1 : Combination of Read/Write
Example 2: Combination of Read/Write
Summary

- Memories provide storage for computers
- Memories are organized in words
  - Selected by addresses
- SRAMs store data in latches
  - Accessed by surrounding circuitry
- RAM waveforms indicate the control signals needed for access
- Words in SRAMs are accessed with decoders
  - Only one word selected at a time